A review on path collisions and resources usage in hybrid optical network on chip (HONoC)

ABSTRACT

System-on-chip (SoC) architectures are getting communication-bound both from physical wiring and distributed computation point of view. Wiring delays are becoming dominating over gate delays, which favors short links. The larger SoC the more probably the overall computation is heterogeneous and localized rather than evenly balanced over the chip. These two factors motivate Network-on-Chip (NoC) that brings the techniques developed for macro-scale, multi-hop networks into a chip. But due to shrinkage of transistors and integration of billions of transistors in a single chip, has made NoC no longer suitable to cater for high latency and demand of bandwidth in a multicore processor environment. Thus they have introduce HONoC (hybrid optical network on chip) to cater for the high latency and demand in bandwidth. There are many research that focus on the area of architecture, routing algorithm and switching strategies in order to make the communication run optimally in HONoC. The purpose of this paper is to evaluate main problems in HONoC. From the evaluation, three main problems has been identified which are path collisions, low resource usage and high power consumption in HONoC.

Keyword: Hybrid optical network on chip; Path collisions; Resources optimization; Routing