**Simulation of a 41-level inverter built by cascading two symmetric cascaded multilevel inverter**


ABSTRACT

The main disadvantage for cascaded multilevel inverter is the high number of switching device it needs in an installation. To reduce total harmonics distortion (THD) of the output waveform, the number of output voltage level has to be increased, hence the higher number of switching devices. This consequently increases the installation cost, inverter size and voltage losses at the load terminals. In this paper a new cascaded multilevel inverter concept is proposed with a small number of switching devices and dc sources needed. The 41-level inverter consist of several high voltage and low voltage dc sources. The switching strategy of the inverter is the low voltage dc sources are switched in several times in a half cycle of the output. The 41-level cascaded multilevel inverter operation is then demonstrated by the Matlab simulation.



**Keyword:** Cascaded multilevel inverter; Low THD; Minimum conducting switches; Reduced switching devices