Sub-picosecond jitter resolution wide range digital delay line for SoC integration

ABSTRACT

A novel three-stage architecture programmable digital delay line (DDL) with a picosecond resolution, 1εs range, and sub-picosecond jitter performance is proposed. Through circuit simulation, a dynamic range of 1εs is obtained in the first stage using 10-bit counters operating at a frequency of 1 GHz. The second stage further refines the delay to 23ps using a tapped inverter chain architecture. Finally, the third stage constructed using a DLL with NAND gate based delay elements further refines the delay step to 1ps resolution with a 0.1ps RMS jitter performance. The proposed digital delay line is designed using a standard 0.13εm Silterra CMOS technology.

Keyword: Delay element; Delay step; Delay-locked loop (DLL); Digital delay line; Dynamic range; Inverter; Jitter; SoC