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A Single DC Source 41-level 115V, 400Hz Cascaded Multilevel Inverter

Ahmad, Syukri Mohamad[1]* and Norman, Mariun[2]

[1]Department of Avionics, Malaysian Institute of Aviation Technology, Universiti Kuala Lumpur, Malaysia
[2]Center for Advance Power and Energy Research, Department of Electric and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia, Malaysia

ABSTRACT

Cascaded multilevel inverters are popular in fields such as oil and gas, power supply installations, and power quality devices. While there are many advantages of the cascaded multilevel inverter, its main disadvantage is the need for large numbers of multiple dc sources. In order to reduce total harmonics distortion (THD) of the output voltage waveform, the amount of output voltage level must be increased, hence the higher number of dc sources. This essentially complicated the inverter design, as most converter transform only one voltage source to another. In this paper a cascaded multilevel inverter topology with a single dc source is discussed. The topology is based on capacitors instead of cells as the multiple voltage sources. The cascaded multilevel inverter topology validity and functionality is verified by the Matlab Simulink simulation of a 100W and 1kW aircraft single phase 41-level inverter.

Keywords: Aircraft inverter, multilevel inverter, total harmonics distortion

INTRODUCTION

Inverters as a power conversion device can be found in three main categories of application; power supply, motor drives and active filters (Tehrani et al., 2011). The multilevel inverter is fast emerging as a popular choice of power inverter in many industries. Compared to two-level systems, multilevel inverter has a better power quality output and low total harmonics distortion (THD) thus providing better power efficiency (Al-Emadi et al., 2016).

Even though the cascaded multilevel inverter has many advantages, the need for multiple dc sources is its setback. In order to reduce the output THD level, the number of output levels need to be increased, and so too the number of dc sources. Apart from this the high number of power switches and related controlling devices makes this model

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E-mail addresses:
ahmadsyukri@unikl.edu.my (Ahmad, Syukri Mohamad),
norman@upk.edu.my (Norman, Mariun)
*Corresponding Author

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unattractive. As the number of output voltage levels are increased, the amount of switching devices are also increased greatly, making the inverter becoming more complex and expensive (Mailah et al, 2009). Although this issue is also important, this paper will only limit the scope of the discussion to only on the issue of multiple dc sources requirement.

AIRCRAFT INVERTER

Onboard inverter became an important part of aircrafts when as aircraft systems became larger and more complex. This is because all these instruments use ac current while the main aircraft power supply at that time comes from 28V dc generator (Hayes & Ray, 1945).

As power electronics device availability increased static inverters became to be the preferred inverter choice for aircraft. The static inverter has no moving parts, the inverter is h more efficient and also smaller and lighter. The common technology is where a 400Hz oscillator is connected to the dc busbar and producing low voltage ac current. The low voltage output then stepped-up using a power transformer to the rated aircraft ac system voltage (Tooley & Wyatt, 2009).

The standard aircraft inverter input and output characteristics are as follows (EASA, 2003):

Input voltage:	28Vdc; tolerance + 2Vdc
Output voltage:	115V ac rms; tolerance +5%, –7%
Frequency:	400Hz; tolerance +1%
Output waveform:	sinusoidal
THD:	less than 7% under all load conditions

THE PROPOSED INVERTER

The nature of a cascaded multilevel inverter operation is the dc sources are stacked on top of one another in series of successions. Care in switching time will create a stepped wave that is almost similar to a clean sinusoidal waveform. The stacked dc sources are connected in series, so the combined voltage output will be similar to a normal ac source.

At any time the inverter is operational dc sources are connected to the load or output terminals, while others may not be used. If the dc sources are replaced with capacitors, when they are not connected to the load, the capacitors can be charged in order to maintain the voltage level of the capacitors.

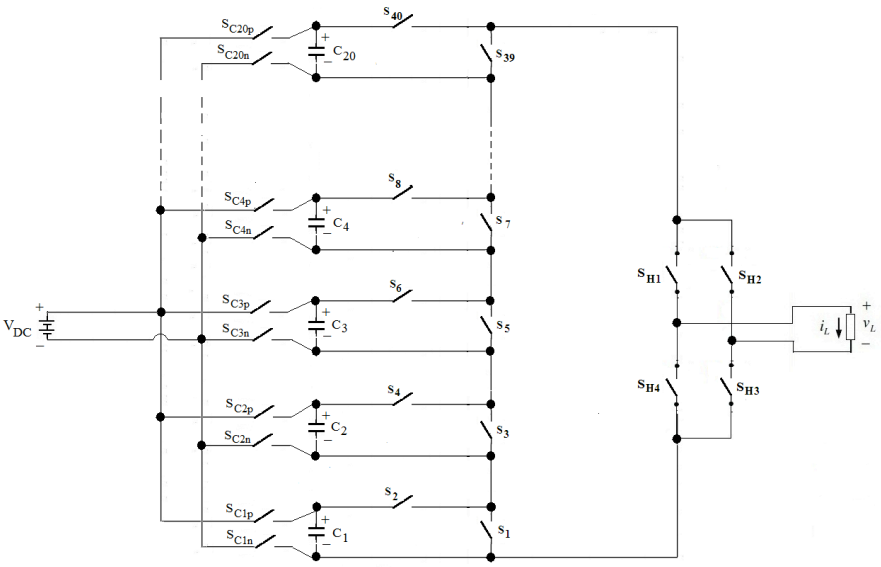

Figure 1. The proposed single dc source cascaded multilevel inverter topology

The proposed single dc source cascaded multilevel inverter topology is shown in Figure 1. The topology is based on the topology proposed by Babei and Hosseini (2009). This topology was chosen because it offers good switches reduction compared to the cascaded H-bridge topology. The topology is then modified by replacing the multiple dc sources with capacitors. The switches arrangement also modified to provide the means to charge the capacitors using a single dc source. The switching states of the switches is shown in Table 1.

Table 1
The switching states of the switches and the resultant output voltage

Charged capacitors	Discharged capacitors	ON switches	OFF switches	Load voltage, VL
C_1, C_2,….C_{19}, C_{20}	-	S_{C1}, S_{C2},..S_{C19}, S_{C20} S_1, S_3,……S_{37}, S_{39} S_{H1}, S_{H3}	S_2, S_4,……S_{38}, S_{40} S_{H2}, S_{H4}	0V
C_2, C_3,…C_{19}, C_{20}	C_1	S_{C2}, S_{C3},..S_{C19}, S_{C20} S_2, S_3,……S_{37}, S_{39} S_{H1}, S_{H3}	S_{C1} S_1, S_4,……S_{38}, S_{40} S_{H2}, S_{H4}	V_{C1}
C_3, C_4,…C_{19}, C_{20}	C_1, C_2	S_{C3}, S_{C4},..S_{C19}, S_{C20} S_2, S_4,……S_{37}, S_{39} S_{H1}, S_{H3}	S_{C1}, S_{C2} S_1, S_3,……S_{38}, S_{40} S_{H2}, S_{H4}	$V_{C1} + V_{C2}$
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•

Table 1
The switching states of the switches and the resultant output voltage (continue)

Charged capacitors	Discharged capacitors	ON switches	OFF switches	Load voltage, VL
C_{19}, C_{20}	C_1, C_2,…C_{17}, C_{18}	S_{C19}, S_{C20} S_2, S_4,……S_{37}, S_{39} S_{H1}, S_{H3}	S_{C1}, S_{C2},..S_{C17}, S_{C18} S_1, S_3,……S_{38}, S_{40} S_{H2}, S_{H4}	V_{C1} + V_{C2} +…. + V_{C17} + V_{C18}
C_{20}	C_1, C_2,…C_{18}, C_{19}	S_{C20} S_2, S_4,……S_{38}, S_{39} S_{H1}, S_{H3}	S_{C1}, S_{C2},..S_{C18}, S_{C19} S=, S_3,……S_{37}, S_{40} S_{H2}, S_{H4}	V_{C1} + V_{C2} +.... + V+ + V_{C19}
-	C_1, C_2,….C_{19}, C_{20}	- S_2, S_4,……S_{38}, S_{40} S_{H1}, S_{H3}	S_{C1}, S_{C2},..S_{C19}, S_{C20} S_1, S_3,……S_{37}, S_{39} S_{H2}, S_{H4}	V_{C1} + V_{C2} +…. + V_{C19} + V_{C20}
C_1, C_2,….C_{19}, C_{20}	-	S_{C1}, S_{C2},..S_{C19}, S_{C20} S_1, S_3,……S_{37}, S_{39} S_{H2}, S_{H4}	- S_2, S_4,……S_{38}, S_{40} S_{H1}, S_{H3}	– 0V
C_2, C_3,…C_{19}, C_{20}	C_1	S_{C2}, S_{C3},..S_{C19}, S_{C20} S_2, S_3,……S_{37}, S_{39} S_{H2}, S_{H4}	S_{C1} S_1, S^4,……S_{38}, S_{40} S_{H1}, S_{H3}	– V_{C1}
C_3, C_4,…C_{19}, C_{20}	C_1, C_2	S_{C3}, S_{C4},..S_{C19}, S_{C20} S_2, S_4,……S_{37}, S_{39} S_{H2}, S_{H4}	S_{C1}, S_{C2} S_1, S_3,……S_{38}, S_{40} S_{H1}, S_{H3}	– (V_{C1} + V_{C2})
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
C_{19}, C_{20}	C_1, C_2,…C_{17}, C_{18}	S_{C19}, S_{C20} S_2, S_4,……S_{37}, S_{39} S_{H2}, S_{H4}	S_{C1}, S_{C2},..S_{C17}, S_{C18} S_1, S_3,……S_{38}, S_{40} S_{H1}, S_{H3}	– (V_{C1} + V_{C2} +.... + V_{C17} + V_{C18})
C_{20}	C_1, C_2,…C_{18}, C_{19}	S_{C20} S_2, S_4,……S_{38}, S_{39} S_{H2}, S_{H4}	S_{C1}, S_{C2},..S_{C18}, S_{C19} S_1, S_3,……S_{37}, S_{40} S_{H1}, S_{H3}	– (V_{C1} + V_{C2} +.... + V_{C18} + V_{C19})
-	C_1, C_2,….C_{19}, C_{20}	S_2, S_4,……S_{38}, S_{40} S_{H2}, S_{H4}	S_{C1}, S_{C2},..S_{C19}, S_{C20} S_1, S_3,……S_{37}, S_{39} S_{H1}, S_{H3}	– (V_{C1} + V_{C2} +.... + V_{C19} + V_{C20})

RESULTS AND DISCUSSION

The performance of the inverter and the validity of the topology are tested using Matlab Simulink simulation. The switching timing are based on the algorithm discussed by Syukri Mohamad and Mariun (2012). Two load conditions are being tested – 100W and 1kW. This is because most of the large commercial aircrafts are equipped with a 1kW rated onboard inverter to provide the emergency power to the essential equipment in the event of emergency and normal power loss.

A 41-level inverter realization based on the proposed cascaded multilevel inverter topology is constructed based on the circuit shown in Figure 1 using Matlab Simulink modelling platform. The choice of power switches is Mosfet because as it has very fast switching time, simple gate circuit, virtually no gate current and negligible gate circuit loss (Rajashekara, 2002).

The inverter is supplied with a controlled single dc source, and the rated output voltage is 115Vrms, 400Hz. Peak voltage is about 163V. The measured parameters are shown in Figure 2 for 100W load condition and Figure 3 for 1kW load condition. Both loads are pure resistive loads.

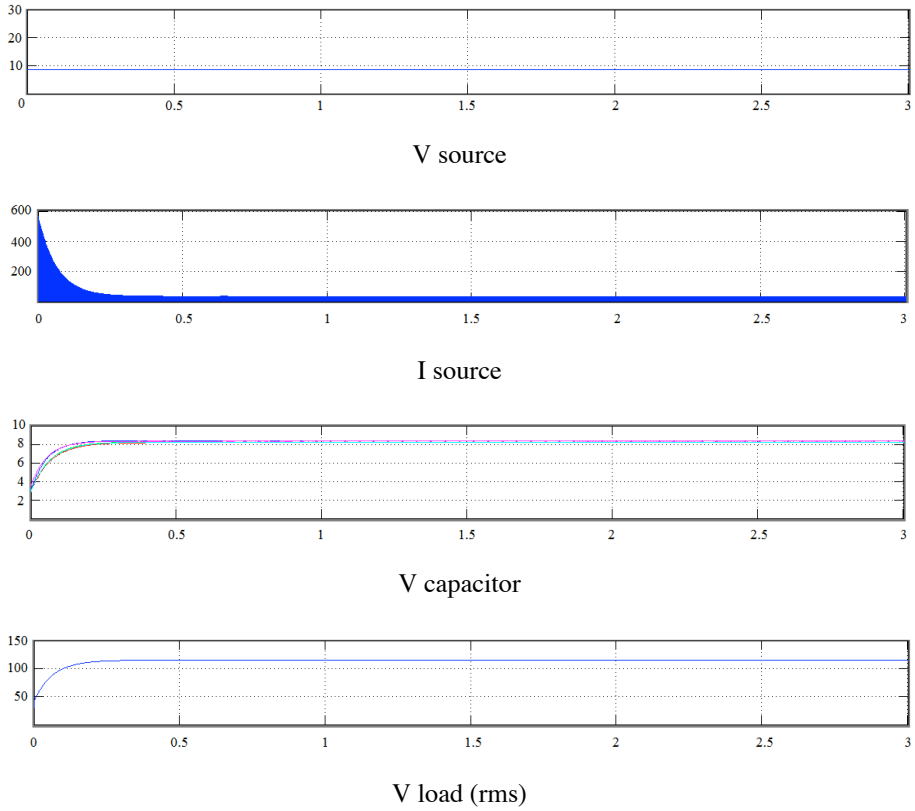

Figure 2. Measured parameters of the inverter when operating with 100W load

For the 100W load condition, the inverter input voltage is around 8.6V and the capacitors used are 12V, 0.12F capacitors. The initial current is very high, as can be expected of the charging process of the uncharged 20 capacitors.

As the capacitors built up the voltages, its current was also reduced to a constant level, with maximum value of 35A and rms value of 16.81A. The rms output voltage is 115V and the output voltage with the input current stabilizes after only about 0.3s.

The output power is measured at 99.95W while the input power is 144.566W, giving the efficiency of the inverter at 69.14%

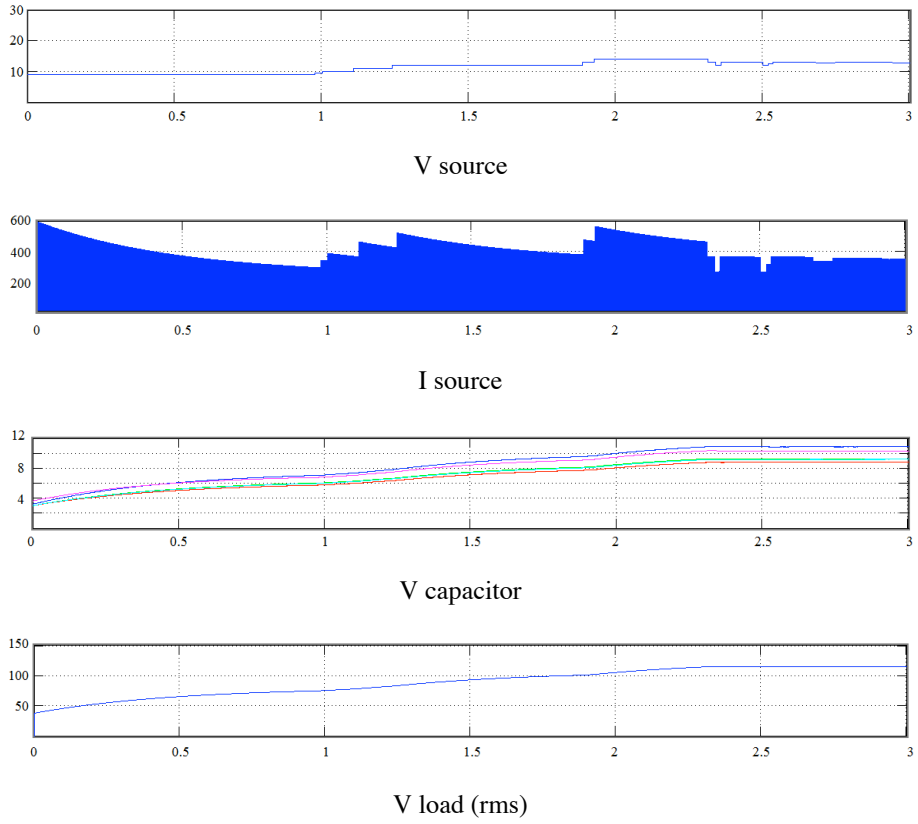

Figure 3. Measured parameters of the inverter when operating with 1kW load

For the 1kW load condition, the inverter input voltage changes around 9V to 14V during initial starting with the input voltage stabilized at 12.85V. The capacitors used are 16V, 1.2F capacitors. The source current fluctuates with the changing input voltage as the capacitors are very sensitive to any sudden voltage changes. The input current stabilizes at around 343A to 344A peak value, with the rms value settles at 165.5A.

As the capacitors built up the voltages, the capacitors voltage settles at a constant level, with values between 8.81V to 10.86V. The rms output voltage is 115V and the output voltage stabilizes after only about 2.3s. The output power is measured at 999.6W while the input power is 2126.675W, giving the efficiency of the inverter at 47.00%. The output waveform of the inverter is almost identical to a clean sinusoidal waveform (see Figure 4). The output THD reading at 100W load is 1.999% while at 1kW load is 3.307%.

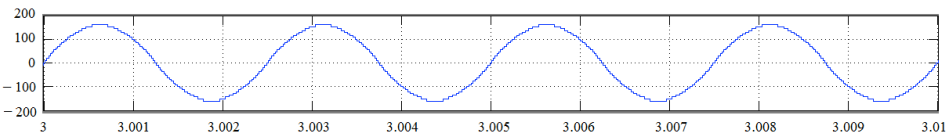

Figure 4. The inverter output voltage waveform

CONCLUSION

A single dc source 41-level aircraft inverter has been successfully developed and constructed using Matlab Simulink modelling platform. The inverter is then simulated with the actual load rating, similar to the load condition of a large commercial aircraft inverter. The parameters are measured and compared to the standard set by aviation authority. The inverter output voltage is 115V rms, 400Hz, conforming with the conditions set out in the aviation standard. The output THD is also well below the 7% limit given in the standard. However, the efficiency of the inverter is relatively poor, with its high input current, . which may be rectified using a dedicated current control method.

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