Efficient low-complexity digital predistortion for power amplifier linearization

ABSTRACT

In this paper, a low-complexity model is proposed for linearizing power amplifiers with memory effects using the digital predistortion (DPD) technique. In the proposed model, the linear, low-order nonlinear and high-order nonlinear memory effects are computed separately to provide flexibility in controlling the model parameters so that both high performance and low model complexity can be achieved. The performance of the proposed model is assessed based on experimental measurements of a commercial class AB power amplifier by applying a single-carrier wideband code division multiple access (WCDMA) signal. The linearity performance and the model complexity of the proposed model are compared with the memory polynomial (MP) model and the DPD with single-feedback model. The experimental results show that the proposed model outperforms the latter model by 5 dB in terms of adjacent channel leakage power ratio (ACLR) with comparable complexity. Compared to MP model, the proposed model shows improved ACLR performance by 10.8 dB with a reduction in the complexity by 17% in terms of number of floating-point operations (FLOPs) and 18% in terms of number of model coefficients.