UNIVERSITI PUTRA MALAYSIA

DESIGN OF A CURRENT CONVEYOR ANALOGUE MULTIPLIER FOR ENERGY METER USING 0.35 µm MIMOS CMOS TECHNOLOGY

NG MIN SHEN

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DESIGN OF A CURRENT CONVEYOR ANALOGUE MULTIPLIER FOR ENERGY METER USING 0.35 µm MIMOS CMOS TECHNOLOGY

By

NG MIN SHEN

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirement for the Degree of Master of Science

December 2007

UPM

DEDICATED TO
MY LATE MOTHER
MADAM KONG SIEW HONG

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

DESIGN OF A CURRENT CONVEYOR ANALOGUE MULTIPLIER FOR ENERGY METER USING 0.35 µm MIMOS CMOS TECHNOLOGY

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December 2007

Chairman: **Professor Sudhanshu Shekhar Jamuar**

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Analogue VLSI circuits are essential in many real-time signal processing applications as naturally occurring signals are analogue. The four-quadrant analogue multiplier is a key building block in analogue signal processing circuits. It is used to construct circuits like the modulator and waveform generator. The ideal output (V_{out}) of a multiplier is related to the inputs by $V_{out} = K_m V_X V_Y$, where K_m is the multiplier gain with units of V^{-1}, and V_X and V_Y are input voltages. In reality, imperfections exist in the multiplier gain, resulting in offsets and nonlinearities. Important parameters such as power dissipation, supply voltage, input dynamic range, bandwidth, total harmonic distortion (THD) and linearity are used to assess the performance of an analogue multiplier.

Nowadays both digital and analogue systems are routinely integrated onto single chips. Digital circuits commonly use low-voltage supply and employ techniques to reduce power consumption. Mixed analogue-digital circuits must be designed to operate in a low-voltage, low-power environment. Conventional analogue multipliers designed with low supply voltage suffer from performance trade-offs, resulting in low bandwidth and low dynamic range because the design of analogue

circuits is a trade-off of various performance parameters such as power dissipation, supply voltage, gain, linearity and noise.

The objective of this research is to design a low-voltage, low-power CMOS analogue multiplier that will address the above problems. The multiplier is designed in a modified bridged-triode scheme (MBTS) and uses current conveyors. As all analogue circuits can be decomposed into several sub-circuits, the performance of these sub-circuits decides the characteristics of the resultant circuit structure. The proposed circuit makes use of the current conveyor's many special features, such as high output impedance and large bandwidth, to construct a low-voltage four-quadrant multiplier.

The analogue multiplier designed in this research operates with a supply voltage of ±1V. The total harmonic distortion obtained from this multiplier is less than two percent, the input operating swing is up to $1V_{pp}$, and the bandwidth achieved is more than 100MHz. It is designed using a 0.35µm technology from the Malaysian Institute of Microelectronics (MIMOS). In addition, an RMS-to-DC converter is designed using the same low-voltage design technique used for designing the adaptively-biased low-voltage current mirror (ABLVCM). Then an energy meter is designed using this analogue multiplier and the RMS-to-DC converter.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

REKA BENTUK PENDARAB ANALOG KONVEYOR ARUS UNTUK METER TENAGA MENGGUNAKAN TEKNOLOGI 0.35 µm CMOS MIMOS

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Litar analog VLSI adalah penting dalam banyak aplikasi pemprosesan isyarat masa nyata kerana isyarat semula jadi adalah bersifat analog. Pendarab analog empat kuadran adalah blok binaan yang amat penting dalam litar pemprosesan isyarat analog. Ia digunakan untuk membina litar seperti pemodulat dan penjana gelombang. Keluaran yang unggul (V_{out}) untuk suatu pendarab boleh dikaitkan kepada masukannya menerusi persamaan $V_{out} = K_m V_X V_Y$, di mana K_m adalah gandaan pendaraban dalam unit V^{-1}, dan V_X serta V_Y adalah voltan masukan dwikutub. Hakikatnya, ketidaksempurnaan wujud dalam gandaan tersebut dan ini mengakibatkan ofset dan ketidaklinearan. Parameter-parameter yang penting seperti pelesapan kuasa, voltan bekalan, julat dinamik masukan, lebar jalur, jumlah herotan harmonik (THD) dan kelinearan digunakan untuk menilai prestasi pendarab analog.

Masa ini kedua-dua sistem digital dan analog lazimnya diintegrasikan ke dalam cip tunggal. Litar digital lazimnya menggunakan voltan bekalan rendah dan pelbagai teknik untuk mengurangkan penggunaan kuasa. Litar campuran analog-digital perlu direka bentuk untuk beroperasi dalam persekitaran voltan dan kuasa rendah. Pendarab analog bervoltan rendah yang direka bentuk secara konvensional akan

terjejas prestasinya kerana wujudnya keseimbangan antara jenis prestasi yang berlainan, lalu mengakibatkan lebar jalur yang terbatas dan julat dinamik yang rendah. Ini berpunca daripada sifat reka bentuk litar analog yang mana parameter-parameter prestasi seperti pelesapan kuasa, voltan bekalan, gandaan, kelinearan dan aras hingar perlu diseimbangkan antara satu sama lain.

Objektif penyelidikan ini ialah reka bentuk suatu pendarab analog CMOS berbekal voltan rendah dan berkuasa rendah yang akan menangani masalah yang telah disebut. Pendarab ini direka bentuk dalam skema perentang triod terubah suai (MBTS) dan ia menggunakan konveyor arus. Oleh kerana kesemua litar analog boleh dipecahkan kepada beberapa sublitar, prestasi sublitar akan menentukan sifat-sifat litar keseluruhan. Litar yang dicadangkan telah mempergunakan ciri-ciri istimewa konveyor arus seperti impedans keluaran yang tinggi dan julat lebar jalur yang besar untuk membina satu pendarab empat kuadran bervoltan rendah.

Pendarab analog yang direka bentuk dalam penyelidikan ini beroperasi dengan bekalan voltan ±1 V. Jumlah herotan harmonik pendarab ini adalah kurang daripada dua peratus, ayunan masukan yang beroperasi sehingga 1 V_{pp} dan julat lebar jalur adalah melebihi 100 MHz. Ia direka bentuk menggunakan teknologi 0.35 μm daripada Institut Mikroelektronik Malaysia (MIMOS). Selain itu, satu penukar RMS-ke-DC telah direka bentuk dengan menggunakan teknik reka bentuk bervoltan rendah yang sama dengan teknik yang digunakan ke atas cermin arus dikawalsuai bervoltan rendah. Penukar RMS-ke-DC digunakan bersama pendarab analog untuk mereka bentuk sebuah meter tenaga.

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I certify that an Examination Committee has met on 31 December 2007 to conduct the final examination of Ng Min Shen on his Master of Science thesis entitled "Design of Current Conveyors Analogue Multiplier for Energy Meter using 0.35 μm MIMOS CMOS Technology" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

NG MIN SHEN

Date: 29 February 2008

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LIST OF ABBREVIATIONS

ABLVCM	Adaptively-Biased Low-Voltage Current Mirror
AC	Alternating Current
BJT	Bipolar Junction Transistor
BSIM	Berkeley Short-Channel IGFET Model
CC	Current Conveyor
CCII+	Second generation class AB current conveyor
CFB	Current-Feedback
CM	Current Mirror
CMC	Current-Mode Circuit
CMOS	Complementary Metal-Oxide Semiconductor
CSF	Complementary Source Follower
DC	Direct Current
EDA	Electronic Design Automation
FG	Floating-Gate
KVL	Kirchhoff's Voltage Law
LVCM	Low-Voltage Current Mirror
MBTS	Modified Bridged-Triode Scheme
MIMOS	Malaysian Institute of Microelectronics
MOS	Metal-Oxide Semiconductor
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
NMOS	*n*-type Metal-Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	*p*-type Metal-Oxide Semiconductor

RMS	Root Mean Square
SNR	Signal-to-Noise Ratio
SPICE	Simulation Programme with Integrated Circuit Emphasis
THD	Total Harmonic Distortion
TSMC	Taiwan Semiconductor Manufacturing Company
VLSI	Very-Large-Scale Integration
VMC	Voltage-Mode Circuit

LIST OF NOTATIONS

α_o	Current conveyor current transfer function
C_{ox}	Gate oxide capacitance per unit area of a MOSFET
f	Frequency
g_{ds}	MOSFET Conductance
g_m	MOSFET Transconductance
γ	MOSFET body effect coefficient
γ_o	Current conveyor voltage transfer function
I_D	MOSFET drain current
I_{intra}	Intra-cell interference
k	Boltzmann's constant
K_m	Multiplier gain
λ	MOSFET channel-length modulation coefficient
L	MOSFET channel length
M	Number of gate fingers of MOSFET
Φ_F	MOSFET bulk electrostatic potential
P	Power
r_o	Resistor that represents the channel length modulation
T	Temperature
μ	Average electron mobility in the channel of a MOSFET
V_{DD}	Positive Supply Voltage
V_{DS}	Drain-source voltage of MOSFET
V_{GS}	Gate-source voltage of MOSFET

V_{pp}	Peak-to-peak voltage
V_{SB}	Source-bulk voltage of MOSFET
V_{SS}	Negative Supply Voltage
V_{TH}	Threshold/overdrive voltage of MOSFET
V_{TH0}	Zero-bias threshold/overdrive voltage of MOSFET
W	MOSFET channel width

CHAPTER 1

INTRODUCTION

Analogue VLSI circuits are essential in many real-time signal processing applications as naturally occurring signals are analogue. They are used in applications such as integrated sensing, image processing, speech recognition, etc. Integrated analogue circuits offer speed, precision, complexity and cost competitiveness over discrete implementation.

The prediction of the demise of analogue electronics over the last decades has proven to be unfounded. Analogue circuit designers continue to be in great demand even as many functions that were traditionally implemented in the analogue domain have migrated into the digital domain now.

This is because the physical world is inherently analogue and analogue circuitry remains absolutely necessary in converting analogue to digital information and vice-versa. As new applications continue to emerge, analogue circuits with their superior performance in speed and power are employed. Wireless communications and artificial neural networks are some examples of mixed system where both digital and analogue circuits are routinely integrated onto single chips. Analogue multipliers are one widely used sub-system in analogue signal processing, which find applications in the modulator, waveform generator, adaptive filters, and even as a weighting synapse in an artificial neural network.

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The increasing demands of mobile devices, such as mobile phones, laptops, hearing aids and pacemakers, necessitate the use of low-power analogue circuits operating with low voltage. Low-power use is essential to ensure reasonable battery life and weight. Even in non-mobile devices, low-power use helps to reduce the size of the heat-removal device. So an important research area for analogue circuitry is the area of low-voltage and low-power design.

1.1 Problem Statements

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The ideal output of a multiplier, shown in Figure 1.1, is related to the inputs by $V_{out} = K_m V_X V_Y$, where K_m is the multiplier gain with units of V^{-1}, and V_X and V_Y are input voltages. In reality, imperfections exist in the multiplier gain, resulting in output offsets and nonlinearities. Power dissipation, supply voltage, input dynamic range, bandwidth, total harmonic distortion (THD) and linearity are other important parameters, which are used to assess the performance of an analogue multiplier.

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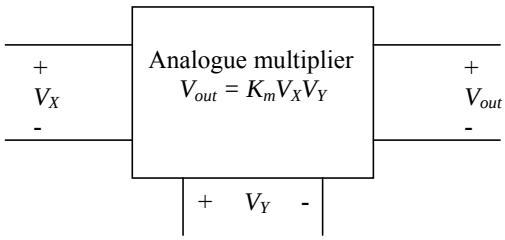

Figure 1.1: Block schematic of a multiplier.

Conventional designs for CMOS analogue multipliers are based on the square-law characteristics of the MOS transistor (Bult & Wallinga, 1986) (Pena-Finol &

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