

Implementation of convolutional encoder and Viterbi decoder using VHDL

ABSTRACT

This work focuses on the realization of convolutional encoder and adaptive Viterbi decoder (AVD) with a constraint length, K of 3 and a code rate (k/n) of $1/2$ using field-programmable gate array (FPGA) technology. This paper presents a 4-state, radix-2, hard decision AVD which has the ability to decode adaptively through different traceback length (TL). The performance of the implemented AVD is analyzed by using ISE 9.2 and MATLAB simulations. The AVD is targeted to a Xilinx XCV300PQ240-4 FPGA device for hardware realization. The decoder parameter TL can be reconfigured via the implementation of AVD, in accordance with the changing channel noise characteristics of the threshold signal-to-noise ratio (SNR), which is 6 dB. The synthesis results show that the reconfiguration parameter TL of 4 and 15 of AVD implementation has significant difference ($>20\%$ improvement) in FPGA device utilization. The results also show that the use of reconfiguration leads to a 28% area occupancy of slice usage improvement over a TL of 15 model compared to a TL of 4 model with tolerable loss of decode accuracy, in accordance with the bit error rate (BER) for real-time voice and video.

Keyword: Convolutional encoder; FPGA; VHDL; Viterbi decoder