



**UNIVERSITI PUTRA MALAYSIA**

***CROSSTALK-AWARE ERROR CONTROL CODING TECHNIQUES  
FOR RELIABLE AND ENERGY EFFICIENT NETWORK ON CHIP***

**WAMEEDH NAZAR FLAYYIH**

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**By**

**WAMEEDH NAZAR FLAYYIH**

**Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia,  
in Fulfilment of the Requirements for the Degree of Doctor of Philosophy**

**August 2014**

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## *DEDICATION*

*To My*

*Wife My Soul Mate*

*Mother Unconditional Love*

*Daughter Light of My Life*

*Father My Role Model*



Abstract of thesis presented to the Senate of Universiti Putra Malaysia  
in fulfilment of the requirement for the degree of Doctor of Philosophy

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**WAMEEDH NAZAR FLAYYIH**

**August 2014**

**Chair: Fakhrol Zaman Rokhani, PhD**

**Faculty: Engineering**

With the continuous downscaling in semiconductor technology more blocks are being integrated in a single chip. Network on Chip (NoC) represents the main solution for the increased on chip communication complexity. One of the major challenges in NoC is the communication reliability due to the small feature sizes, high operating frequency and low operating voltage of the chips. Achieving reliable operation under the influence of deep-submicron noise sources including crosstalk noise at low voltage operation is a major challenge for network on chip links.

In this work, new joint coding schemes are proposed to provide high level of protection from errors and simultaneously reduce the crosstalk induced bus delay. The proposed coding schemes are based on wire duplication and simple parity checks calculated over the rows and columns of the two-dimensional data. This Duplicated Two-Dimensional Parities (DTDP) coding provides high Hamming distance allowing high error protection capability. In addition, the duplication technique addresses crosstalk delay effects allowing higher bus frequency operation. The high error protection capability enables the reduction of wires operating voltage while maintaining the target reliability level, leading to power/energy savings.

For a given Hamming distance, providing only error detection without correction provides the highest possible protection. Accordingly, the first proposed coding scheme is based on automatic repeat request (ARQ) policy providing up to seven errors detection, thus named DTDP-7ED. On the other hand, the second proposed coding scheme is based on hybrid ARQ (HARQ) policy. Single error correction capability is added to reduce the retransmission probability which comes on the cost of reduced error detection capability, resulting in single error correction and six error detection (DTDP-SEC6ED). The two proposed schemes allow for higher reduction in voltage swing as compared to other joint coding schemes which reflects into higher power savings. Since DTDP-7ED has the highest error detection which results into the lowest voltage swing, it achieved the highest power savings. On the other hand, DTDP-SEC6ED achieved lower energy consumption and higher performance.

We also propose a coding scheme that jointly provides crosstalk delay reduction and adaptable error protection according to noise severity. This was motivated by the inefficient energy consumption of traditional designs that constantly work assuming worst case noise scenario. The scheme works in one of three modes by duplicating the data bits, the data bits and one-dimensional parities, or the data bits and two-dimensional parities at low, intermediate, and high noise conditions respectively. The maximum protection mode achieves 51.1% energy savings over Duplicate Add Parity (DAP) coding scheme. This energy savings is increased to 59.5% and 63.0% at intermediate and low protection modes respectively. This comes with a comparable area and maximum frequency compared to other similar coding schemes.



Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

**TEKNIK-TEKNIK PENGEKODAN KAWALAN RALAT  
BERKESEDARAN-TUTURSILANG UNTUK KETEGUHAN DAN TENAGA  
YANG CEKAP DALAM RANGKAIAN PADA CIP**

By

**WAMEEDH NAZAR FLAYYIH**

**Ogos 2014**

**Pengerusi: Fakhrul Zaman Rokhani, PhD**  
**Fakulti: Kejuruteraan**

Kesinambungan daripada skalaturun dalam teknologi semikonduktor, lebih blok disepadu dalam satu cip tunggal. Rangkaian atas Cip (NoC) mewakili penyelesaian utama bagi kerumitan komunikasi cip yang meningkat. Salah satu cabaran utama dalam NoC adalah kebolehpercayaan komunikasi, ini kerana ciri saiz kecil, frekuensi operasi yang tinggi dan voltan operasi cip-cip yang rendah. Mencapai kebolehpercayaan operasi di bawah pengaruh sumber hingar dalam-submikron termasuk hingar tutursilang pada operasi voltan rendah adalah satu cabaran besar bagi rangkaian pada penghubung cip.

Dalam penyelidikan ini, skim pengkodan sama yang baru dicadangkan untuk menyediakan tahap perlindungan yang tinggi daripada ralat dan serentak mengurangkan tutursilang yang menyebabkan kelewatan bas. Skim pengkodan yang dicadangkan adalah berdasarkan penduaan wayar dan pemeriksaan pariti mudah dikira sepanjang baris dan lajur dalam data dua dimensi. Pengkodan Pariti Penduaan Dua Dimensi (DTDP) ini menyediakan jarak Hamming yang tinggi membolehkan keupayaan pengesanan/pembetulan ralat yang tinggi. Di samping itu, teknik penduaan itu menangani kesan-kesan tutursilang pada kelewatan isyarat yang membolehkan frekuensi operasi bas yang lebih tinggi. Keupayaan pengesanan/pembetulan ralat yang tinggi membolehkan pengurangan voltan operasi pada wayar-wayar di samping mengekalkan tahap kebolehpercayaan yang disasarkan, yang membawa kepada penjimatan kuasa/tenaga.

Untuk jarak Hamming yang diberikan, menyediakan pengesanan ralat sahaja tanpa pembetulan memberikan perlindungan paling tinggi. Sehubungan itu, cadangan pertama skim pengkodan adalah berdasarkan kepada dasar permintaan berulang automatik (ARQ) berupaya mengesan sehingga tujuh ralat, dengan itu ia dinamakan DTDP-7ED. Sebaliknya, skim cadangan kedua pengkodan adalah berdasarkan kepada dasar ARQ hibrid (HARQ). Keupayaan pembetulan ralat tunggal ditambah untuk mengurangkan kebarangkalian penghantaran semula yang mengurangkan keupayaan pengesanan ralat, menghasilkan pembetulan ralat tunggal dan enam pengesanan ralat (DTDP-SEC6ED). Kedua-dua skim dicadangkan membolehkan

pengurangan yang lebih tinggi dalam ayunan voltan berbanding dengan skim-skim pengekodan bersama lain, yang mencerminkan kepada simpanan kuasa yang lebih tinggi. Sejak DTDP-7ED mempunyai pengesanan ralat yang paling tinggi yang menyebabkan voltan ke dalam buaian yang paling rendah, ia mencapai penjimatan kuasa tertinggi. Sebaliknya, DTDP-SEC6ED mencapai penggunaan tenaga yang lebih rendah dan prestasi yang lebih tinggi.

Kami juga mencadangkan satu skim pengekodan yang bersama menyediakan pengurangan kelewatan tutursilang dan perlindungan ralat disesuaikan mengikut tahap hingar. Ini didorong oleh penggunaan tenaga yang tidak cekap daripada reka bentuk tradisional yang sentiasa bekerja dengan mengandaikan senario hingar yang paling buruk. Skim ini berfungsi di salah satu daripada tiga mod dengan menggandakan bit data, bit data dan pariti satu dimensi, atau bit data dan pariti dua dimensi masing-masing pada keadaan hingar yang rendah, pertengahan dan tinggi. Mod perlindungan maksimum mencapai 51.1% penjimatan tenaga lebih berbanding skim pengkodan Penduaan Tambah Pariti (DAP). Penjimatan tenaga meningkat kepada 59.5% pada mod perlindungan pertengahan dan 63.0% pada mod perlindungan rendah. Ini dilengkapi dengan kawasan yang setanding dan kekerapan maksimum berbanding dengan skim-skim pengekodan sama yang lain.



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I certify that a Thesis Examination Committee has met on 21 – August – 2014 to conduct the final examination of Wameedh Nazar Flayyih on his thesis entitled "Crosstalk-Aware Error Control Coding Techniques for Reliable and Energy Efficient Network on Chip" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

Members of the Thesis Examination Committee were as follows:

**Abd. Rahman bin Ramli, PhD**

Associate Professor  
Faculty of Engineering  
Universiti Putra Malaysia  
(Chairman)

**Roslina binti Mohd Sidek, PhD**

Associate Professor  
Faculty of Engineering  
Universiti Putra Malaysia  
(Internal Examiner)

**M. Iqbal bin Saripan, PhD**

Associate Professor  
Faculty of Engineering  
Universiti Putra Malaysia  
(Internal Examiner)

**Magdy A. Bayoumi, PhD**

Professor  
Faculty of Engineering  
University of Louisiana at Lafayette  
United States  
(External Examiner)

---

**NORITAH OMAR, PhD**

Associate Professor and Deputy Dean  
School of Graduate Studies  
Universiti Putra Malaysia

Date: 18 August 2014

This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

**Fakhrul Zaman Rokhani, PhD**

Senior Lecturer  
Faculty of Engineering  
Universiti Putra Malaysia  
(Chairman)

**Khairulmizam Samsudin, PhD**

Senior Lecturer  
Faculty of Engineering  
Universiti Putra Malaysia  
(Member)

**Shaiful Jahari Hashim, PhD**

Senior Lecturer  
Faculty of Engineering  
Universiti Putra Malaysia  
(Member)

---

**BUJANG BIN KIM HUAT, PhD**

Professor and Dean  
School of Graduate Studies  
Universiti Putra Malaysia

Date:

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Signature: \_\_\_\_\_

Signature: \_\_\_\_\_

Name of  
Chairman of  
Supervisory

Committee: Fakhrul Zaman Rokhani

Name of  
Member of  
Supervisory

Committee: Khairulmizam Samsudin

Signature: \_\_\_\_\_

Name of  
Member of  
Supervisory

Committee: Shaiful Jahari Hashim



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