Design of a reconfigurable FFT processor using multi-objective genetic algorithm

ABSTRACT

This paper describes the implementation of Multi-objective Genetic Algorithm (MOGA) in a 16-point Radix-4 Single Path Delay Feedback (R4SDF) pipelined Fast Fourier Transform (FFT) processor in Verilog. The role of MOGA is to optimize the wordlength of the FFT coefficient and at the same time make sure the processor operates at acceptable Signal to Noise Ratio (SNR). Reducing the wordlength of FFT coefficient will contribute to lower Switching Activity (SA), thus lower power consumption is required for the operation of FFT processor.

Keyword: FFT processor; Signal to noise ratio; Switching activity