Reduced hardware architecture for energy-efficient IoT healthcare sensor nodes

ABSTRACT

Healthcare solutions through the introduction of wearable healthcare devices are benefitting from Internet of Things technology. Though these small form-factor wearable devices promise great benefits, guaranteeing long device operating lifetime is yet the biggest challenge due to high-energy consumption. In this paper, a reduced hardware architecture system-on-chip targeting digital block design was proposed higher energy efficiency. The design has been verified by synthesizing into FPGA and implemented in silicon based on Silterra 180nm process. Results show that the proposed design achieved reduction up to 24% of leakage power and 15% of dynamic power reduction over reference design. In addition, 24.3% of excessive area was reduced by using the proposed reduced hardware architecture technique.

Keyword: ASIC; Energy-efficient; FPGA; Internet of Things; Microcontroller