
UNIVERSITI PUTRA MALAYSIA

# DUAL-SAMPLING SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER IMPLEMENTATION IN FIELD-PROGRAMMABLE GATE ARRAY

MOHD SYAHRIL BIN NOOR SHAH

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**By**

**MOHD SYAHRIL BIN NOOR SHAH**

**Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia in Fulfillment of the Requirements for the Degree of Master of Science**

**July 2013**

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**Dedication**

**TO MY BELOVED WIFE, SONS, FAMILIES AND FRIENDS**

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirements for the degree of Master of Science

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With the latest advancement in field-programmable gate array (FPGA) technology, the analog-to-digital converter (ADC) can now be integrated within the FPGA digital fabric without the need for an external ADC chip. Realization of the ADC is possible by utilizing the low voltage differential signaling (LVDS) pin pair available on the FPGA chip along with some external passive components. The implementation of ADC in the FPGA chip has a few advantageous where the cost, board space and components are reduced. The FPGA no longer needs an external ADC to be integrated with the analog interfaces.

FPGA implementation of ADC structures such as successive approximation register (SAR) and sigma-delta ADC are considered and their performances are evaluated. In a close loop digital controller application such as motor controller, it requires a fast ADC conversion to drive a motor with a quick feedback response. SAR ADC is capable of fast conversion time while the sigma-delta ADC sacrifices a fast

conversion time for accuracy. However, the SAR ADC conversion contains errors in FPGA implementation and sigma-delta ADC is too slow for a practical close loop system.

A dual-sampling sigma-delta (DSSD) ADC is proposed utilizing the potential of the sigma-delta ADC and maximizing the usage of FPGA. The proposed ADC is capable of sampling both clock edges instead of the conventional single edge sampling. The sampled analog signal is feedback through an RC filter network which will be tracked and compared with the analog input signal. The result for each clock edges are summed to obtain the final converted digital word. Thus, the workload is distributed since the sampling data is divided into two clock edges. It allows faster data processing and maximizing data throughput. The aim of this research is to reduce the ADC conversion time while maintaining the quality of the signal converted. The performance of the DSSD ADC is compared with other ADC structures implemented in FPGA.

The performance of the proposed ADC structure is written in verilog hardware description language (HDL) and evaluated using the Altera Cyclone II FPGA chip on a Development and Education (DE) II board. The results show the proposed 8-bit DSSD ADC with 27 MHz sampling clock provides the ADC with 1 least significant bit (LSB) error, 4.8 μs conversion time and a bandwidth of 104.1 kHz. The DSSD ADC structure has improved from the conventional sigma-delta structure which is 3 LSBs, 9.4 μs conversion time and bandwidth of 53.2 kHz.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

**PELAKSANAAN DWI-PENSAMPELAN PENUKAR ANALOG-KE-DIGITAL SIGMA-DELTA DALAM TATASUSUNAN GET BOLEH ATUR CARA-MEDAN**

Oleh

**MOHD SYAHRIL BIN NOOR SHAH**

**Julai 2013**

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Dengan kemajuan terkini dalam teknologi tatasusunan get boleh atur cara medan (FPGA), penukar analog ke digital (ADC) kini boleh disepadukan dalam persekitaran digital FPGA tanpa keperluan cip ADC luaran. Adalah mungkin untuk merealisasikan ADC dengan menggunakan sepasang pin isyarat perbezaan voltan rendah (LVDS) yang terdapat pada cip FPGA dengan beberapa komponen-komponen pasif luaran. Pelaksanaan ADC dalam cip FPGA lebih memberi kebaikan kerana dapat mengurangkan kos, ruang papan dan komponen. FPGA tidak lagi bergantung kepada mana-mana ADC luaran untuk berintegrasi dengan perantaraan muka analog.

Pelaksanaan FPGA dengan struktur-stuktur ADC seperti daftar penghampiran berturutan (SAR) dan ADC sigma-delta dipertimbangkan dan prestasinya dinilai. Dalam aplikasi pengawal digital gelung tutup seperti pengawal motor memerlukan penukaran ADC yang cepat supaya dapat memandu motor dengan sambutan suap balik yang cepat. ADC SAR mampu memberikan penukaran masa yang cepat

manakala ADC sigma-delta mengorbankan masa penukaran cepat untuk ketepatan. Walau bagaimanapun, penukaran SAR ADC mengandungi ralat-ralat dalam pelaksanaan FPGA dan ADC sigma-delta adalah terlalu lambat untuk sistem gelung tutup praktikal.

Sebuah ADC dwi-pensampelan sigma-delta (DSSD) adalah dicadangkan untuk menggunakan potensi ADC sigma-delta dan untuk memaksimumkan penggunaan FPGA. ADC yang dicadangkan mampu membuat persampelan di kedua-dua pinggir jam daripada pensampelan pinggir tunggal yang biasa. Isyarat analog yang disampel disuap balik melalui rangkaian penapis RC yang akan dikesan dan dibandingkan dengan isyarat masukan analog. Hasil bagi setiap pinggir jam dijumlahkan untuk mendapatkan perkataan digital yang akhir. Oleh itu, beban kerja teragih disebabkan data telah tebahagi kepada dua pinggir jam. Ia membolehkan data diproses dengan lebih cepat dan memaksimumkan pemprosesan data. Tujuan kajian ini adalah untuk mengurangkan masa penukaran ADC disamping mengekalkan kualiti isyarat yang ditukar. Prestasi ADC DSSD dibandingkan dengan struktur-struktur ADC yang lain bagi pelaksanaan dalam FPGA.

Prestasi struktur ADC yang dicadangkan ditulis dalam bahasa verilog penerangan perkakasan (HDL) dan dinilai menggunakan cip FPGA Altera Cyclone II pada papan pembanggunan dan pendidikan (DE) II. Keputusannya menunjukkan ADC 8-bit yang dicadangkan dengan jam persampelan 27 MHz memberikan ralat keluaran 1 bit paling kecil (LSB), masa penukaran 4.78 μs dan lebar jalur 105.2 kHz. Struktur DSSD ADC telah menambah baik struktur sigma-delta yang lazim iaitu 3 LSBs, masa penukaran 9.4 μs dan lebar jalur 53.2 kHz.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Master of Science. The members of the Supervisory Committee were as follows:

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## DECLARATION

I declare that the thesis is my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or other institutions.

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