**Power consumption optimization technique in ACS for space time trellis code viterbi decoder**

ABSTRACT

To provide fast digital communications systems, energy efficient, high-performance, low power is critical for decoding mobile receiver device. This paper proposes a low power optimization techniques in the Add Compare Select (ACS) unit for Space Time trellis codes (STTC) Viterbi decoder. STTC Viterbi decoder is used as a reference case. This paper discusses about how to lower the power in the ACS architecture, to optimize the Viterbi decoder STTC in reducing the total power consumption. Based on the results of design and analysis, power consumption Viterbi decoder modeling, low power system for STTC Viterbi decoder is proposed. Design and optimization of ACS unit in STTC Viterbi decoding is done using Verilog HDL language. Power analysis tools in the software Altera Quartus 2 is used for the synthesis of total system power consumption. Optimization strategy showed an increase of 83% power reduction compared to previous studies.

**Keyword:** Power consumption; Space time trellis code; Viterbi decoder