UNIVERSITI PUTRA MALAYSIA

DESIGN OF SEGMENTED 14-BIT LOW POWER CURRENT STEERING DIGITAL TO ANALOG CONVERTER

SOLMAZ RASTEGAR MOGHADDAM MANSOURI

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By

SOLMAZ RASTEGAR MOGHADDAM MANSOURI

Thesis Submitted to the School of Graduate Studies, University Putra Malaysia, in Fulfillment of the Requirements for the Degree of Master of Science

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Dedicated to
My dearest parents
For their extensive love
and
Their endless care

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

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Chairman: **Izhal B. Abdul Halin, D.Eng**

Faculty: **Engineering**

Digital to Analog Converter (DAC) function is to convert a given string of digital input into an analog voltage or current value. Due to its functionality, DACs is considered an essential system used to interface between digital and analog systems. The past few decades have seen many methods of realizing DAC circuits such as the resistive ladder networks, binary-weighted structure, pulse-width modulators, thermometer-coded architecture and hybrid structures. These implementations have yielded high resolution and high performance DACs that find application generally in consumer electronics, automotive industry and even in the medical field. For example video signal processing and wireless communications

apply DACs capable of handling data at speeds of several hundreds of mega samples per second with a resolution of 12 to 14 bits.

According to literature, majority of the advanced DACs used in these devices concentrate on low power architectures. To achieve low power, they utilize current-steering circuits consisting of either the binary-weighted structure, thermometer-coded (unary) architecture or by taking the advantage of both methods in a segmented DAC architecture. For any given digital input code, the current steering circuits are responsible for generating the analog output value and are also responsible for static power dissipation. However, available DACs do not focus on reducing the static power dissipation. Moreover, static power dissipation will rise as future applications must demand for higher resolution DACs which translate to an increase in current sources that dissipate even more static power.

This work proposes a method to address the static power dissipation of a high-resolution 14-bit DAC. The DAC consists of a digital module and an analog module. The analog module consists of switched current sources and arrays of current cells which contribute much to static power dissipation. To allow for low static power dissipation, unselected current sources are put in hibernation mode. In this mode the cells operate at half of their nominal currents. Towards this end, the transistors in the current sources still operate in the saturation region but at half their nominal current which translates to a reduction in static power dissipation.

On the other hand, the digital module is designed using latch circuits, thermometer decoder circuits and latency equalizer circuits. This work also highlights the novel design and simulation of the latency equalizer circuit that is used to synchronize different segments of the DAC during its operation. This circuit introduces delays to currents generated from the many current cells in order for them to arrive simultaneously at the current summing node. The design is optimized in order for the DAC to operate at a speed of 100MHz.

As a proof of concept, the TSMC 0.18μm technology is used to design and simulate the DAC. It is shown that a 50% reduction of current in hibernation mode which is from 256 μA to 128μA, allows the total power dissipation of the DAC to be 25mW at an operation speed of 100MHz. Functionality simulation reveal that the designed DAC has an INL and DNL of less than 0.5 LSB, respectively. When compared to specifications of similar DACs in literature, the total power consumption of this DAC which is approximately 25mW exhibits approximately 69% improved power dissipation.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

REKABENTUK DALAM SEGMEN 14-BIT KUASA PEMANDU ARUS RENDAH PENUKAR DIGITAL KE ANALOG

Oleh

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April 2011

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Penukar digital ke analog (DAC) adalah untuk menukar rentetan data digital kepada voltan analog atau arus. Oleh kerana fungsinya, DACs dianggap satu sistem yang penting digunakan untuk berhubung antara sistem digital dan analog. Beberapa dekad yang lalu telah menyaksikan banyak kaedah litar DAC direalisasikan seperti rangkaian tangga perintang, struktur berwajaran binari, modular nadi-lebar, senibina termometer berkod dan struktur hibrid. Ini telah menghasilkan pelaksanaan resolusi tinggi dan DACs prestasi tinggi yang diaplikasikan secara amnya dalam elektronik, industri automotif dan juga dalam bidang perubatan. Sebagai contoh pemprosesan isyarat video dan komunikasi tanpa wayar memerlukan DACs yang mampu mengendalikan data pada kelajuan beberapa ratusan mega sampel sesaat dengan resolusi 12 hingga 14 bit.

Menurut kajian terdahulu, majoriti DACs digunakan dalam alat-alat ini memberi tumpuan kepada seni bina yang kuasa rendah. Untuk mencapai kuasa yang rendah, mereka menggunakan litar current-steering yang terdiri daripada sama ada struktur berwajaran binari, seni bina termometer berkod (unari) atau menggabungkan dengan menggunakan kelebihan daripada kedua-dua kaedah dalam senibina DAC yang berlainan. Untuk mana-mana kod input digital yang diberikan, litar current-steering bertanggungjawab untuk menghasilkan nilai output analog dan juga bertanggungjawab untuk pelesapan kuasa statik. Walau bagaimanapun, DACs yang sedia ada tidak memberi tumpuan kepada mengurangkan pelesapan kuasa statik. Selain itu, pelesapan kuasa statik akan meningkat sejajar dengan aplikasi pada masa depan yang menuntut untuk menggunakan DACs yang beresolusi lebih tinggi atau bermaksud peningkatan dalam sumber arus yang melesapkan lebih kuasa statik.

Penyelidikan ini mencadangkan satu kaedah untuk menangani masalah pelesapan kuasa statik dalam 14-bit DAC beresolusi tinggi. DAC ini terdiri daripada modul digital dan modul analog. Modul analog terdiri daripada sumber arus dan barisan sel arus yang menyumbang banyak kepada pelesapan kuasa statik. Bagi membolehkan pelesapan kuasa statik rendah, sumber arus yang tidak dipilih akan dimasukkan ke dalam mod hibernasi. Dalam mod ini, sel beroperasi pada separuh daripada arus nominalnya. Bagi tujuan ini, transistor dalam sumber arus masih beroperasi di kawasan ‘saturation’ tetapi pada separuh arus nominalnya yang membawa maksud kepada pengurangan dalam pelesapan kuasa statik.

Sebaliknya, modul digital direka dengan menggunakan litar selak, litar penyahkod

termometer dan litar penyamaan latency. Karya ini juga memaparkan reka bentuk baru dan simulasi litar penyamaan latency yang digunakan untuk menyelaras pelbagai segmen DAC semasa operasinya. Litar ini memperkenalkan kelewatan untuk arus yang dijana daripada banyak sel arus bagi membolehkan mereka untuk tiba serentak pada nod jumlah arus. Reka bentuk ini dioptimumkan supaya DAC beroperasi pada kelajuan 100MHz.

Sebagai bukti konsep, teknologi 0.18µm TSMC digunakan untuk reka bentuk dan simulasi DAC. Ia menunjukkan bahawa pengurangan arus sebanyak 50% dalam mod hibernasi iaitu dari 256 µA kepada 128µA, membolehkan pelupusan kuasa pada DAC sebanyak 25mW pada kelajuan operasi 100MHz. Simulasi fungsi mendedahkan bahawa DAC direka mempunyai setiap INL dan DNL kurang daripada 0.5 LSB. Jika dibandingkan dengan DACs berspesifikasi sama dalam kajian terdahulu, jumlah penggunaan kuasa dalam DAC ini dalam lingkungan 25mW kira-kira 69% kuasa pelesapan telah diperbaiki .

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I certify that an Examination Committee has met on to conduct the final examination of Solmaz Rastegar Moghaddam Mansouri on her Master of Science thesis " Design Of Segmented 14-Bit Low Power Current Steering Digital To Analog Converter " in accordance with Universiti and University Colleges Act 1971 and the Constitution of the Universiti Putra[P.U.(A) 106] 15 March 1998. The Committee recommends that the candidate be awarded the relevant degree.

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citation which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently submitted for any other degree at Universiti Putra Malaysia or other institutions.

SOLMAZ RASTEGAR MOGHADDAM MANSOURI

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TABLE OF CONTENTS