UNIVERSITI PUTRA MALAYSIA

INVESTIGATION AND STATISTICAL SIMULATION OF VARIATION AWARE 14 nm SRAM CACHE MEMORY ARCHITECTURE

SOMAYEH RAHIMI POUR

FK 2011 121

INVESTIGATION AND STATISTICAL SIMULATION OF VARIATION AWARE 14 nm SRAM CACHE MEMORY ARCHITECTURE

By

SOMAYEH RAHIMI POUR

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Master of Science

October 2011

DEDICATION

This thesis is dedicated to my lovely parents who gave me best supports by their hearts. I would also like to dedicate this work to my beloved husband who gave me confidence and accompanied me in all difficulties.

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master.

INVESTIGATION AND STATISTICAL SIMULATION OF VARIATION AWARE 14 nm SRAM CACHE MEMORY ARCHITECTURE

By
SOMAYEH RAHIMI POUR

October 2011

Chairman: Khairulmizam Samsudin, PhD

Faculty: Engineering

Aggressive technology scaling to 14 nm technology node increases variability in transistors performance and introduces serious reliability challenges to the design of microprocessors. This creates several challenges in building reliable systems from transistors with unpredictability of delay. Scaling increases the impact of intrinsic parameter fluctuation on the yield and functionality of SRAM cache. Since a large fraction of chip area is devoted to on-chip caches, it is important to protect these SRAM structures against failures. The intrinsic parameter fluctuation within a cache can lead to variability in the behavior of the different transistors and is the most noticeable type of variation that resulting in a violation of delay requirements and uncertainty. These variations have an increasing impact on cache performance and yield because the transistors used in cache are among the minimal size for each particular technology generation.

This work introduces a systematic simulation methodology to investigate the impact of intrinsic parameter fluctuations on cache important parameters. The cache performance is evaluated in terms of cache hit ratio and cache miss penalty. This methodology captures the intrinsic parameter fluctuations information from

circuit level and provides essential link between circuit-level simulation and system-level simulation. In order to study the impact of intrinsic parameter fluctuations on important cache parameters, the percentage of accesses that result in cache miss (cache miss ratio), in the presence of different source of intrinsic parameter fluctuations is investigated. Cache misses happen when the required data for reading or writing is not in the cache or there is an access time failure. However, as the electrical parameters of the transistors are prone to intrinsic fluctuations, the access time varies from memory cell to memory cell. When the access time of a cell is longer than the maximum tolerable limit (T_{MAX}), an access time failure is said to have occurred, and that cell considered as a faulty cell. A systematic analysis of the effects of random discrete dopants, body thickness variations and line edge roughness on a 25 nm, 20 nm and 14 nm technology node is performed. From systems point of view, the intrinsic parameter fluctuations must be captured in behavioral level which can be used in system simulators like Icarus Verilog HDL. The impact of intrinsic parameter fluctuations on cache miss penalty time causes significantly failures in cache performance. Therefore, it is important to consider alternative cache architectures that are more tolerable to intrinsic parameter fluctuations. A new variation aware cache architecture is proposed to reduce the impact of the intrinsic parameter fluctuations in cache in nanoscale regime. This technique enables TLB to access just the non faulty words with negligible area overhead. Experimental results on a 32K fully associative L1 cache show that the proposed architecture can achieve 85% reduction in cache miss penalty.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master sains.

PENYIASATAN DAN SIMULASI BERSTATISTIK SENI BINA CACHE MEMORI 14 nm SEDAR PERUBAHAN

Oleh
SOMAYEH RAHIMI POUR

Oktober 2011

Pengerusi: Khairulmizam Samsudin, PhD

Fakulti: Kejuruteraan

Penskalaan agresif sehingga 14 nm nod teknologi meningkatkan kebolehubahan dalam prestasi transistor dan memperkenalkan cabaran keboleharapan yang serius kepada reka bentuk mikropemproses. Ini mewujudkan beberapa cabaran dalam membina sistem yang boleh dipercayai dari transistor dengan ketidaktentuan lengah. Penskalaan meningkatkan kesan perubahan parameter hakiki pada hasil dan fungsi cache SRAM. Oleh kerana sebahagian besar kawasan cip ditumpukan kepada cache atas-cip, ia adalah penting untuk melindungi struktur SRAM terhadap kegagalan. Fluktuasi parameter hakiki dalam cache boleh membawa kepada kebolehubahan dalam tingkah laku transistor yang berbeza dan yang paling ketara jenis perubahan yang menyebabkan pelanggaran keperluan kelewatan dan ketidakpastian. Perbezaan-perbezaan ini mempunyai kesan yang mendalam kepada prestasi dan hasil cache kerana transistor yang digunakan di dalam cache adalah diantara yang bersaiz minimum bagi setiap generasi teknologi tertentu. Tesis ini memperkenalkan metodologi simulasi yang sistematik bagi menyiasat kesan perubahan parameter hakiki pada parameter-parameter cache yang penting. Prestasi cache dinilai dari segi nisbah kena cache dan penalti tidak kena cache. Metodologi ini

membolehkan pengumpulan parameter perubahan maklumat hakiki dari paras litar terhasil dan menyediakan pertalian penting antara simulasi peringkat-litar dan simulasi peringkat-sistem. Untuk mengkaji kesan perubahan parameter hakiki pada parameter-parameter penting cache, peratusan akses yang mengakibatkan cache tidak kena, dalam kehadiran sumber yang berlainan perubahan parameter hakiki turut disiasat. Cache tidak kena berlaku apabila data yang diperlukan untuk membaca atau menulis tidak berada di dalam cache atau kegagalan masa akses. Walau bagaimanapun, parameter elektrik transistor terdedah kepada perubahan hakiki, maka masa akses berbeza dari setiap sel memori kepada sel memori yang lain. Apabila masa akses sel lebih panjang daripada had maksimum yang boleh diterima(T_{MAX}), kegagalan masa akses dikatakan telah berlaku, dan sel itu dianggap sebagai sel yang rosak. Satu analisis yang sistematik kesan rawak pendopan diskret, variasi ketebalan badan dan kekasaran garis pinggir pada nm 25, 20 nm dan 14 nm teknologi nod telah dilakukan. Dari sudut pandangan sistem, fluktuasi parameter hakiki mesti ditangkap pada tahap tingkah laku di mana ia boleh digunakan dalam sistem simulasi seperti Icarus Verilog HDL. Kesan perubahan parameter hakiki terhadap masa penalti cache tidak kena menyebabkan kegagalan yang ketara dalam prestasi cache. Oleh itu, ia adalah penting untuk mempertimbangkan seni bina cache alternatif yang boleh menerima perubahan terhadap parameter hakiki. Variasi baru seni bina cache yang sedar telah dicadang untuk mengurangkan kesan perubahan parameter hakiki dalam cache dalam rejim berskala nano. Teknik ini membolehkan TLB mengakses perkataan yang tidak rosak dengan overhed kawasan yang boleh diabaikan. Keputusan eksperimen ke atas cache L1 berkapasiti 32K yang bersekutu sepenuhnya menunjukkan bahawa seni bina yang dicadangkan boleh mencapai pengurangan 85% terhadap penalti tidak kena cache.

ACKNOWLEDGEMENTS

From the formative stages of this, to the final draft, I owe an immense debt of gratitude to my supervisor, Dr. Khairulmizam b. Samsudin senior Lecturer of the Department of Computer and Communication Systems Engineering, Faculty of Engineering, Universiti Putra Malaysia. I also would like to say thank to Dr Fakhrul Zaman Bin Rokhani, the senior lecturer of Department of Computer and Communication Systems Engineering, my supervisory committee member who supports me to do this research with his valuable advise scientifically in different steps.

I wish to extend my warmest thanks to all those who have helped me with my work in the Department of Computer and Communication Systems Engineering.

I am indebted for the help and unconditional love provided to me by my lovely parents. My special gratitude is due to my dear friends who assisting me with this work.

I certify that a Thesis Examination Committee has met on 17 Oct 2011 to conduct the final examination of Somayeh Rahimi Pour on her thesis entitled "Investigation and Statistical Simulation of Variation Aware 14 nm SRAM Cache Memory Architecture" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

Members of the Thesis Examination Committee were as follows:

Abdul Rahman b. Ramli, PhD
Associate Professor
Faculty of Graduate Studies
Universiti Putra Malaysia
(Chairman)

Shaiful Jahari b. Hashim, PhD
Lecturer
Faculty of Graduate Studies
Universiti Putra Malaysia
(Internal Examiner)

Roslina Binti Mohd Sidek, PhD
Associate Professor
Faculty of Graduate Studies
Universiti Putra Malaysia
(Internal Examiner)

Othman bin Sidek, PhD
Associate Professor
Faculty of Graduate Studies
Universiti Putra Malaysia
Malaysia
(External Examiner)

_____

BUJANG KIM HUAT, PhD
Professor and Deputy Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the **Master of Science**. The members of the Supervisory Committee were as follows:

Khairulmizam Samsudin, PhD
Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Fakhrul Zaman Rokhani, PhD
Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Member)

_____

BUJANG BIN KIM HUAT, PhD
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

DECLARATION

I declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or at any other institutions.

_____

SOMAYEH RAHIMI POUR

Date: 17 October 2011

TABLE OF CONTENTS