DESIGN OF A 1.8V SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER WITH LOW NOISE

HUR A. HASSAN

FK 2010 53
DESIGN OF A 1.8V SUCCESSIVE APPROXIMATION REGISTER
ANALOG-TO-DIGITAL CONVERTER WITH LOW NOISE

By
HUR A. HASSAN

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Master of Science

September 2010
Dedicated to

My dearest Parents, My Wife, My Brothers and Sisters

For their extraordinary love and endless care
Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

DESIGN OF A 1.8V SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER WITH LOW NOISE

By

HUR A. HASSAN

September 2010

Chairman: Izhal Abdul Halin, PhD

Faculty: Engineering

The purpose of this thesis is to design a 1.8V 8-bit resolution Successive Approximation Register Analog to Digital Converter (SAR-ADC) that has low flicker noise performance. SAR-ADC circuit is one of the most frequently used circuits in many applications. Some application suffers from noise signals at low frequencies, for example in sensors which are used in Compressed Natural Gas Direct Injection (CNGDI). Analog designers constantly deal with the problem of noise since it is related to linearity, power dissipation and speed.

The main building blocks of the SAR-ADC consist of the Sample-and-Hold (S/H) Circuit, comparator, control logic unit and a Digital to Analog Converter (DAC). This research focuses on the design of the S/H circuit as it is the greatest contributor to flicker noise. The S/H circuit in this research uses a bootstrapped CMOS switch that allows for improved accuracy. To reduce flicker noise, two types of amplifiers are proposed to be incorporated in the design of the S/H circuit, namely the two stage
operational amplifier and the folded cascode amplifier. After comparison between
the two in terms of noise performance, the S/H employing the two stage amplifier is
chosen for the SAR-ADC design. Moreover, this structure provides high stability,
and rail to rail input signal.

Results from detailed simulation confirm that the SAR-ADC has low flicker noise.
From simulation, input referred noise for both two stage operational amplifier and
folded cascode amplifier are 18 nV/√Hz. The output noise for the folded cascode op-
amp is 191µv/√Hz, while the two stage op-amp has output noise 36 µv/√Hz. Since
the S/H circuit using the two stage amplifier has output noise less than that of the
folded cascode operational amplifier, it is chosen for the design of the SAR-ADC
operating at low frequencies (1Hz to 500 KHz). From simulation, the SAR-ADC
employing the two stage S/H circuit shows sampling speeds of 1 MS/s, DNL at 0.45
LSB, INL at 0.58 LSB, SNR of 48 dB, power dissipation of 252 µW and an ENOB
of 7.68-bit. All simulations were done in 0.18µm TSMC CMOS process technology.
Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

PERANCANGAN PENDEKATAN A 1.8 V BERTURUT-TURUT REGISTER ANALOG KE DIGITAL CONVERTER NOISE DENGAN RENDAH

Oleh

HUR A. HASSAN

September 2010

Pengerusi: Izhal Abdul Halin, PhD

Fakulti: Kejuruteraan

Tujuan tesis ini adalah untuk merekabentuk sebuah penukar analog ke digit 8-bit jenis pendaftar aproksimasi berturutan (SAR-ADC) dengan prestasi hingar kerlipan yang rendah dan beropearasi pada 1.8V. SAR-ADC adalah litar yang paling kerap digunakan dalam pelbagai aplikasi. Sesetengah aplikasi mengalami gangguan hingar dalam isyarat pada frekuensi yang rendah antaranya adalah seperti pada pengesan yang digunakan didalam suntikan secara langsung gas asli padat (CNGDI) untuk mengawal fungsi enjin kereta. Perek analog kerap berdepan dengan masalah hingar memandangkan ianya berkaitan dengan lelurusan, disipasi kuasa dan kelajuan. Penyelidikan ini akan memperkenalkan reka bentuk SAR-ADC dengan prestasi kerlipan bunyi yang rendah. Binaan utama SAR-ADC terdiri daripada blok litar sampel dan pegang (S/H), pembanding, unit kawalan logik dan penukar digit ke analog (DAC). Kajian ini menumpu kepada rekabentuk litar S/H oleh kerana ianya penyumbang terbesar kepada hingar kerlipan. Litar S/H dalam kajian ini menggunakan suis bootstrap CMOS yang dapat memperbaiki ketepatan litar S/H.
Untuk mengurangkan hingar kerlipan, dua jenis penguat operasi CMOS dicadangkan dalam binaan litar S/H iaitu penguat operasi dua tahap dan penguat operasi folded cascode. Selepas perbandingan yang dibuat antara keduanya dari sudut prestasi hingar, litar S/H menggunakan penguat operasi dua tahap telah dipilih untuk mereka bentuk SAR-ADC. Tambahan lagi, strukutur ini membenarkan kadar penguatan tinggi dan juga masukan isyarat rel ke rel.

Keputusan yang diperolehi dari simulasi secara terperinci telah mengesahkan reka bentuk SAR-ADC dengan prestasi hingar kerlipan yang rendah untuk tesis ini. Dari simulasi, hingar masukan untuk kedua-dua penguat operasi dua tahap dan penguat operasi folded cascode adalah sebanyak 18 nV/√Hz. Keluaran hingar untuk penguat operasi folded cascode adalah 191µv/√Hz, manakala penguat operasi dua tahap mempunyai keluaran hingar sebanyak 36 µv/√Hz. Oleh kerana litar S/H dengan menggunakan penguat operasi dua tahap mempunyai keluaran hingar lebih rendah daripada yang menggunakan penguat operasi folded cascode, ianya telah dipilih untuk rekabentuk SAR-ADC yang beroperasi pada julat frekuensi yang rendah (1Hz sehingga 500 KHz). SAR-ADC yang telah disimulasi menggunakan penguat operasi dua tahap menunjukkan kelajuan sampel sebanyak 1 MS/s dengan DNL sebanyak 0.45LSB, INL sebanyak 0.58 LSB, SNR sebanyak 48 dB, disipasi kuasa sebanyak 252µW dan ENOB sebanyak 7.68-bit. Semua simulasi telah dilakukan menggunakan proses teknologi 0.18µm TSMC CMOS.
ACKNOWLEDGMENTS

In the name of Allah, the Most Beneficent, the Most Merciful

I would like to express my thanks to my supervisor, Dr. Izhal, for his guidance and advice throughout my research. He taught me how to be a researcher with his wonderful personality. I ask Allah to keep him safe, and support him with good health and the power to help students with his expert knowledge and scientific abilities.

I would like also to extend my thanks to members of my committee for their service: A. P. Dr. Ishak and A. P. Dr. Roslina for their moral and academic assistance.

My gratitude also goes to all my colleagues in the Electrical laboratory for their encouragement and helpful advice.

Finally, I would like to thank my family for their unconditional care from birth to this stage of my life and study, for without their continuous support and precious prayers I would not have been able to do my research. I know their blessings will always be with me in all my endeavours and I dedicate this success to them. Thanks, my beloved family.
I certify that an Examination Committee met on 10/8/2010 to conduct the final examination of Hur Abd Al Reda Hassan on his Master of Science thesis, “DESIGN OF A 1.8V SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER WITH LOW NOISE” in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that the candidate be awarded the relevant degree.

Members of the Examination Committee are as follows:

**Samsul Bahari b. Mohd. Noor, PhD**
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

**Roslina bt. Mohd. Sidek, PhD**
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

**Dr. Nasri b. Sulaiman, PhD**
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

**Razali b. Ismail, PhD**
Professor
Faculty of Engineering
Universiti Teknologi Malaysia
(External Examiner)

---

**BUJANG KIM HUAT, PhD**
Professor and Deputy Dean
School Of Graduate Studies
Universiti Putra Malaysia

Date:
This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Master of Science. The members of the Supervisory Committee were as follows:

Izhal Abdul Halin, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Ishak b. Aris, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Member)

HASANAH MOHD GHAZALI, PhD
Professor and Dean
School Of Graduate Studies
Universiti Putra Malaysia

Date: October 2010
DECLARATION

I declare that the thesis is my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently submitted for any other degree at Universiti Putra Malaysia or other institutions.

Hur Abd Al Reda Hassan

Date: 30/09/2010
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEDICATION</td>
<td>ii</td>
</tr>
<tr>
<td>ABSTRACT</td>
<td>iii</td>
</tr>
<tr>
<td>ABSTRAK</td>
<td>v</td>
</tr>
<tr>
<td>ACKNOWLEDGMENTS</td>
<td>vi</td>
</tr>
<tr>
<td>APPROVAL</td>
<td>viii</td>
</tr>
<tr>
<td>DECLARATION</td>
<td>x</td>
</tr>
<tr>
<td>LIST OF TABLES</td>
<td>xiii</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>xiv</td>
</tr>
<tr>
<td>LIST OF ABBREVIATIONS</td>
<td>xvi</td>
</tr>
</tbody>
</table>

## CHAPTER

### 1 INTRODUCTION
1.1 Motivation 4  
1.2 Problem Statement 4  
1.3 Research Objectives 5  
1.4 Scope of Work 5  
1.5 Thesis layout 6

### 2 LITERATURE REVIEW
2.1 Introduction 7  
2.2 Overview on Analog to Digital Converter 7  
2.3 Fundamentals of Analog to Digital Conversion 8  
2.4 Types of Analog to Digital Converters 10  
2.4.1 Flash ADC 10  
2.4.2 Pipelined ADC 10  
2.4.3 Cyclic ADC 11  
2.4.4 Sigma Delta \( \Sigma \Delta \) ADC 11  
2.4.5 SAR-ADC 12  
2.5 SAR-Architecture 12  
2.6 Sample-and-Hold Circuit 15  
2.6.1 Spectra of Sampled Signals 15  
2.6.2 Sample-and-Hold Architecture 16  
2.7 Operational Amplifier 18  
2.7.1 Output Voltage Swing 19  
2.7.2 DC Gain and Phase Margin 19  
2.7.3 Slew Rate 19  
2.8 Comparator 20  
2.9 Digital to Analog Converter 22  
2.10 Switches 24  
2.11 Noise in SAR-ADC 25  
2.11.1 Quantization Noise 25  
2.11.2 Thermal Noise 27  
2.11.3 Flicker Noise 28  
2.12 Summary 34
# RESEARCH METHODOLOGY AND DESIGN

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Introduction</td>
<td>35</td>
</tr>
<tr>
<td>3.2</td>
<td>SAR Architecture and Conversion Principle</td>
<td>36</td>
</tr>
<tr>
<td>3.3</td>
<td>Sample-and-Hold Design</td>
<td>38</td>
</tr>
<tr>
<td>3.4</td>
<td>Selected Op-Amp's Performance</td>
<td>41</td>
</tr>
<tr>
<td>3.4.1</td>
<td>Two Stage Op-Amp Design</td>
<td>42</td>
</tr>
<tr>
<td>3.4.2</td>
<td>Folded Cascode Op-Amp Design</td>
<td>45</td>
</tr>
<tr>
<td>3.5</td>
<td>Flicker Noise Analysis</td>
<td>47</td>
</tr>
<tr>
<td>3.5.1</td>
<td>Noise in Two Stage Op-Amp</td>
<td>49</td>
</tr>
<tr>
<td>3.5.2</td>
<td>Noise in Folded Cascode Op-Amp</td>
<td>52</td>
</tr>
<tr>
<td>3.6</td>
<td>Comparator Design</td>
<td>54</td>
</tr>
<tr>
<td>3.7</td>
<td>Successive Approximation Register</td>
<td>57</td>
</tr>
<tr>
<td>3.8</td>
<td>Digital to Analog Converter Design</td>
<td>59</td>
</tr>
<tr>
<td>3.9</td>
<td>SAR-ADC Architecture</td>
<td>62</td>
</tr>
<tr>
<td>3.10</td>
<td>Performance Measurement Methods</td>
<td>64</td>
</tr>
<tr>
<td>3.10.1</td>
<td>Differential Non-Linearity (DNL)</td>
<td>64</td>
</tr>
<tr>
<td>3.10.2</td>
<td>Integral Non-Linearity (INL)</td>
<td>65</td>
</tr>
<tr>
<td>3.10.3</td>
<td>Signal to Noise Ratio (SNR)</td>
<td>66</td>
</tr>
<tr>
<td>3.11</td>
<td>Summary</td>
<td>67</td>
</tr>
</tbody>
</table>

# MEASURED RESULT AND ANALYSIS

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Introduction</td>
<td>68</td>
</tr>
<tr>
<td>4.2</td>
<td>Experimental Setup</td>
<td>68</td>
</tr>
<tr>
<td>4.3</td>
<td>Sample-and-Hold Simulation Result</td>
<td>69</td>
</tr>
<tr>
<td>4.4</td>
<td>Selected Op-Amp's Performance Simulation Results</td>
<td>72</td>
</tr>
<tr>
<td>4.4.1</td>
<td>Two Stage Op-Amp</td>
<td>72</td>
</tr>
<tr>
<td>4.4.2</td>
<td>Folded Cascode Op-Amp</td>
<td>75</td>
</tr>
<tr>
<td>4.5</td>
<td>Flicker Noise Analysis</td>
<td>77</td>
</tr>
<tr>
<td>4.5.1</td>
<td>Two Stage Op-Amp Noise Result</td>
<td>77</td>
</tr>
<tr>
<td>4.5.2</td>
<td>Folded Cascode Op-Amp Noise Result</td>
<td>80</td>
</tr>
<tr>
<td>4.6</td>
<td>Comparator Simulation</td>
<td>83</td>
</tr>
<tr>
<td>4.7</td>
<td>Successive Approximation Register Simulation</td>
<td>84</td>
</tr>
<tr>
<td>4.8</td>
<td>Digital to Analog Converter Simulation</td>
<td>85</td>
</tr>
<tr>
<td>4.9</td>
<td>SAR-ADC Architecture Simulation Results</td>
<td>86</td>
</tr>
<tr>
<td>4.10</td>
<td>Power Consideration</td>
<td>89</td>
</tr>
<tr>
<td>4.11</td>
<td>Performance Measurements Result</td>
<td>89</td>
</tr>
<tr>
<td>4.11.1</td>
<td>Differential Non-Linearity (DNL)</td>
<td>90</td>
</tr>
<tr>
<td>4.11.2</td>
<td>Integral Non-Linearity (INL)</td>
<td>90</td>
</tr>
<tr>
<td>4.11.3</td>
<td>Signal to Noise Ratio (SNR)</td>
<td>91</td>
</tr>
<tr>
<td>4.12</td>
<td>Comparison with Previous Research</td>
<td>92</td>
</tr>
<tr>
<td>4.13</td>
<td>Summary</td>
<td>94</td>
</tr>
</tbody>
</table>

# CONCLUSION

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>Tasks Conducted to Accomplish the Objectives</td>
<td>96</td>
</tr>
<tr>
<td>5.2</td>
<td>Limitations and Suggestions for Future Research</td>
<td>97</td>
</tr>
</tbody>
</table>

REFERENCES | 98
APPENDIXES | 103
BIODATA OF STUDENT | 107
LIST OF PUBLICATIONS | 107