UNIVERSITI PUTRA MALAYSIA

DESIGN OF A 1.8V SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER WITH LOW NOISE

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By

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Master of Science

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Dedicated to

My dearest Parents, My Wife, My Brothers and Sisters

For their extraordinary love and endless care

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

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The purpose of this thesis is to design a 1.8V 8-bit resolution Successive Approximation Register Analog to Digital Converter (SAR-ADC) that has low flicker noise performance. SAR-ADC circuit is one of the most frequently used circuits in many applications. Some application suffers from noise signals at low frequencies, for example in sensors which are used in Compressed Natural Gas Direct Injection (CNGDI). Analog designers constantly deal with the problem of noise since it is related to linearity, power dissipation and speed.

The main building blocks of the SAR-ADC consist of the Sample-and-Hold (S/H) Circuit, comparator, control logic unit and a Digital to Analog Converter (DAC). This research focuses on the design of the S/H circuit as it is the greatest contributor to flicker noise. The S/H circuit in this research uses a bootstrapped CMOS switch that allows for improved accuracy. To reduce flicker noise, two types of amplifiers are proposed to be incorporated in the design of the S/H circuit, namely the two stage

operational amplifier and the folded cascode amplifier. After comparison between the two in terms of noise performance, the S/H employing the two stage amplifier is chosen for the SAR-ADC design. Moreover, this structure provides high stability, and rail to rail input signal.

Results from detailed simulation confirm that the SAR-ADC has low flicker noise. From simulation, input referred noise for both two stage operational amplifier and folded cascode amplifier are 18 nV/√Hz. The output noise for the folded cascode op-amp is 191μv/√Hz, while the two stage op-amp has output noise 36 μv/√Hz. Since the S/H circuit using the two stage amplifier has output noise less than that of the folded cascode operational amplifier, it is chosen for the design of the SAR-ADC operating at low frequencies (1Hz to 500 KHz). From simulation, the SAR-ADC employing the two stage S/H circuit shows sampling speeds of 1 MS/s, DNL at 0.45 LSB, INL at 0.58 LSB, SNR of 48 dB, power dissipation of 252 μW and an ENOB of 7.68-bit. All simulations were done in 0.18μm TSMC CMOS process technology.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

PERANCANGAN PENDEKATAN A 1.8 V BERTURUT-TURUT REGISTER ANALOG KE DIGITAL CONVERTER NOISE DENGAN RENDAH

Oleh

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Tujuan tesis ini adalah untuk merekabentuk sebuah penukar analog ke digit 8-bit jenis pendaftar aproksimasi berturutan (SAR-ADC) dengan prestasi hingar kerlipan yang rendah dan beropearasi pada 1.8V. SAR-ADC adalah litar yang paling kerap digunakan dalam pelbagai aplikasi. Sesetengah aplikasi mengalami gangguan hingar dalam isyarat pada frekuensi yang rendah antaranya adalah seperti pada pengesan yang digunakan didalam suntikan secara langsung gas asli padat (CNGDI) untuk mengawal fungsi enjin kereta. Pereka analog kerap berdepan dengan masalah hingar memandangkan ianya berkaitan dengan lelurusan, disipasi kuasa dan kelajuan. Penyelidikan ini akan memperkenalkan reka bentuk SAR-ADC dengan prestasi kerlipan bunyi yang rendah. Binaan utama SAR-ADC terdiri daripada blok litar sampel dan pegang (S/H), pembanding, unit kawalan logik dan penukar digit ke analog (DAC). Kajian ini menumpu kepada rekabentuk litar S/H oleh kerana ianya penyumbang terbesar kepada hingar kerlipan. Litar S/H dalam kajian ini menggunakan suis bootstrap CMOS yang dapat memperbaiki ketepatan litar S/H.

Untuk mengurangkan hingar kerlipan, dua jenis penguat operasi CMOS dicadangkan dalam binaan litar S/H iaitu penguat operasi dua tahap dan penguat operasi folded cascode. Selepas perbandingan yang dibuat antara keduanya dari sudut prestasi hingar, litar S/H menggunakan penguat operasi dua tahap telah dipilih untuk mereka bentuk SAR-ADC. Tambahan lagi, strukutur ini membenarkan kadar penguatan tinggi dan juga masukan isyarat rel ke rel.

Keputusan yang diperolehi dari simulasi secara terperinci telah mengesahkan reka bentuk SAR-ADC dengan prestasi hingar kerlipan yang rendah untuk tesis ini. Dari simulasi, hingar masukan untuk kedua-dua penguat operasi dua tahap dan penguat operasi folded cascode adalah sebanyak 18 nV/√Hz. Keluaran hingar untuk penguat operasi folded cascode adalah 191µv/√Hz, manakala penguat operasi dua tahap mempunyai keluaran hingar sebanyak 36 µv/√Hz. Oleh kerana litar S/H dengan menggunakan penguat operasi dua tahap mempunyai keluaran hingar lebih rendah daripada yang menggunakan penguat operasi folded cascode, ianya telah dipilih untuk rekabentuk SAR-ADC yang beroperasi pada julat frekuensi yang rendah (1Hz sehingga 500 KHz). SAR-ADC yang telah disimulasi menggunakan penguat operasi dua tahap menunjukkan kelajuan sampel sebanyak 1 MS/s dengan DNL sebanyak 0.45LSB, INL sebanyak 0.58 LSB, SNR sebanyak 48 dB, disipasi kuasa sebanyak 252µW dan ENOB sebanyak 7.68-bit. Semua simulasi telah dilakukan menggunakan proses teknologi 0.18µm TSMC CMOS.

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I certify that an Examination Committee met on 10/8/2010 to conduct the final examination of Hur Abd Al Reda Hassan on his Master of Science thesis, "DESIGN OF A 1.8V SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL CONVERTER WITH LOW NOISE" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that the candidate be awarded the relevant degree.

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DECLARATION

I declare that the thesis is my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently submitted for any other degree at Universiti Putra Malaysia or other institutions.

Hur Abd Al Reda Hassan

Date:30/09/2010

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