UNIVERSITI PUTRA MALAYSIA

DESIGN OF FIELD PROGRAMMABLE GATE ARRAY-BASED PROPORTIONAL-INTEGRAL-DERIVATIVE FUZZY LOGIC CONTROLLER WITH TUNABLE GAIN

ZEYAD ASSI OBAID

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By

ZEYAD ASSI OBAID

Thesis submitted to the School of Graduate Studies of Universiti Putra Malaysia, in fulfillment of the requirement for the Degree of Master of Science

March 2010

DEDICATIONS

I dedicate this work to the soul of **My Father** (*the Martyr*), who took my hand and taught me the meaning of life, have excelled in guiding me to the correct path of ethics and how to deal with the people. My dear father, i hope Allah (*Sobhanahu wata'la*) that makes the great paradise your door, and make you live with the great and the prophets, and to give you the status of martyrs and I ask Allah (*Sobhanahu wata'la*) enable us to live together in this paradise (*Amen*). My dear father, I will carry this until the end of my life, and move them to my children after me (*Insha'Allah*).

I also dedicate this work to the flower of my life, **My Dear Mother**, the greatest mother in this world. **My dear Mother**, these are the hardest years in my life because I am away from you, I miss you so much. There are no words in this world enough to tell you, just, **I love you.**

Abstract of the thesis presented to the School of Graduate Studies of University Putra Malaysia in the fulfillment of the requirement for the Degree of Master of science

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ZEYAD ASSI OBAID

Mac 2010

Chairman: Nasri Sulaiman, PhD

Faculty: Engineering

Many of fuzzy control applications require real-time operation; higher density programmable logic devices such as Field Programmable Gate Array (FPGA) can be used to integrate large amounts of logic in a single IC. This thesis presents a design of improved Proportional-Integral-Derivative Fuzzy Logic Controller (PIDFC) with tunable gains method using FPGA.

The PIDFC is designed as a PDFC and PIFC connected in parallel through a summer. To simplify the controller design, the PIFC is designed by accumulating the output of the PDFC. The benefits of doing so are twofold, as the number of rules that have to be written is reduced from 512 rules to 64 rules, and depending on two external signals, the controller is able to work as a PDFC, PIFC or PIDFC. The tuning gain block is designed at each input/output stage. This block involves a tuning via scaling the universe of discourse and is able to accept optimal scaling gains. The particle swarm optimization

method (PSO) is used to obtain the optimal values of these gains. PIDFC is designed using VHDL language for implementation on FPGA device, and to employ the improved fuzzy algorithm that offer higher processing speed versus low utilization of chip resource.

Two versions of the PIDFC are designed; the first one is 8-bits FPGA-based controller (8FBC), while the second one is 6-bits (6FBC) version for each inputs/output variables. To test the design, five case studies are used to test the controller in simulation environments in ModelSim and Matlab. The same design is coded in Matlab environment (MSBC) to enable a comparison with the FPGA-based design (FBC). PIDFC needs 16 clock cycles to complete one action. The simulation results showed that the 8FBC is superior to the 6FBC and its responses are much closer to or better to the MSBC or the results in the literature. 8FBC is able to produce an action in 0.3 μs after input latching with maximum frequency of 40 MHz. Therefore, the PIDFC will be able to control a wide range of the systems with high sampling rate.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

DESAIN PERANCANGAN BERBASIS PROGRAMMABLE GATE ARRAY PROPORSIONAL-INTEGRAL-DERIVATIF FUZZY LOGIC CONTROLLER DENGAN GAIN MERDU

Oleh

ZEYAD ASSI OBAID

Marc 2010

Pengerusi: Nasri Bin Sulaiman, PhD

Fakulti : Kejuruteraan

Banyak aplikasi kawalan fuzzy memerlukan operasi real-time; kepadatan lebih tinggi peranti programmable logic seperti array gerbang Gelanggang programmable (FPGA) boleh digunakan untuk mengintegrasikan logik jumlah besar dalam IC tunggal. Tesis ini menyajikan suatu kaedah dikembangkan untuk merancang pengawal logik proporsional-integral-derivatif fuzzy (PIDFC) dengan kaedah keuntungan merdu menggunakan FPGA.

The PIDFC direka sebagai PDFC dan PIFC disambungkan secara selari melalui musim panas. Untuk menyederhanakan desain controller, yang PIFC direka dengan mengumpulkan output dari PDFC. Manfaat melakukannya ada dua, kerana jumlah peraturan yang harus ditulis berkurang dari 512 Peraturan dengan 64 peraturan, dan bergantung pada dua isyarat luaran, controller boleh bekerja sebagai PDFC, PIFC atau

PIDFC. Keuntungan Blok tuning direka pada setiap input / output tahap. Blok ini melibatkan tuning melalui skala alam semesta dari wacana dan boleh menerima keuntungan yang optimum scaling. Zarah kaedah pengoptimuman berkelompok (PSO) digunakan untuk mendapatkan nilai yang optimum daripada keuntungan. PIDFC direka menggunakan bahasa VHDL untuk pelaksanaan pada peranti FPGA, dan menggunakan teknik fuzzy algoritma baru yang menawarkan kelajuan pemprosesan yang lebih tinggi berbanding rendahnya pemanfaatan sumber daya cip.

Dua versi dari PIDFC direka, yang pertama adalah 8-bit berasaskan FPGA kontroler (8FBC), sedangkan yang kedua adalah 6-bit (6FBC) versi untuk setiap input / output variable. Untuk menguji desain, Lima kajian kes digunakan untuk menguji controller dalam lingkungan simulasi di ModelSim dan Matlab. Desain yang sama dikodekan dalam lingkungan Matlab (MSBC) untuk membolehkan perbandingan dengan desain berasaskan FPGA (FBC). PIDFC memerlukan 16 kitaran clock untuk menyelesaikan satu tindakan. Keputusan simulasi menunjukkan bahawa 8FBC adalah lebih unggul dari 6FBC dan responnya jauh lebih dekat atau lebih baik kepada MSBC atau keputusan dalam sastera. 8FBC mampu menghasilkan tindakan dalam 0.3 μs selepas input menempel dengan frekuensi maksimum 40 MHz. Oleh kerana itu, PIDFC akan mampu mengendalikan pelbagai sistem dengan sampling rate tinggi.

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I certify that a Thesis Examination Committee has met on **23 March 2010** to conduct the final examination of Zeyad Assi Obaid on his thesis entitled "**Design of Field Programmable Gate Array-Based Proportional-Integral-Derivative Fuzzy Logic Controller with Tunable Gain**" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the Student be awarded the Master of Science.

Members of the Thesis Examination Committee were as follows:

Senan Mahmod Abdullah, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Roslina Bt. Mohd Sidek, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Samsul Bahari Mohd Noor, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Rubiyah Yusof, PhD
Professor
Center for Artificial Intelligence and Robotics (CAIRO)
Faculty of Engineering
Universiti Teknologi Malaysia
(External Examiner)

BUJANG KIM HUAT, PhD
Professor and Deputy Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of **Master of Science**. The members of the Supervisory Committee were as follows:

Nasri B Sulaiman, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Mohammad Hamiruce b. Marhaban, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Member)

Mohd Nizar B Hamidon, PhD
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Member)

_____
HASANAH MOHD GHAZALI, PhD
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

DECLARATION

I declare that the thesis is my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or at any other institution.

ZEYAD ASSI OBAID

Date:

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