Transistor sizing methodology for low noise charge sensitive amplifier with input transistor working in moderate inversion

ABSTRACT

In this paper noise contribution of current source transistors and sizing methodology in charge sensitive amplifier for application in the front-end readout electronics is presented. In modern deep-submicron technologies, MOS transistor operating region tends to shift from strong inversion to moderate inversion, this makes traditional square-law MOS device modeling not applicable anymore. Thus a simplified EKV model, which is quite successful in all CMOS operating regions, has been adopted to develop a new analytical methodology to optimize geometry of current source transistors so that the noise contribution from these transistors is only a fraction of input transistor noise. A charge sensitive amplifier based on dual PMOS cascode structure is designed by adopting this current source transistor sizing methodology, and has been simulated using 130nm CMOS technology. The proposed methodology and noise contribution from current source transistors have been found in good agreement with simulation results using deep-submicron CMOS technology.

Keyword: CSA; EKV model; Noise optimization