Fabrication and simulation of single crystal p-type Si nanowire using SOI technology

ABSTRACT

Si nanowires (SiNWs) as building blocks for nanostructured materials and nanoelectronics have attracted much attention due to their major role in device fabrication. In the present work a top-down fabrication approach as atomic force microscope (AFM) nanolithography was performed on Si on insulator (SOI) substrate to fabricate a single crystal p-type SiNW. To draw oxide patterns on top of the SOI substrate local anodic oxidation was carried out by AFM in contact mode. After the oxidation procedure, an optimized solution of 30 wt.% KOH with 10 vol.% IPA for wet etching at 63°C was applied to extract the nanostructure. The fabricated SiNW had 70ï 85 nm full width at half maximum width, 90 nm thickness and 4 ε m length. The SiNW was simulated using Sentaurus 3D software with the exact same size of the fabricated device. Iï V characterization of the SiNW was measured and compared with simulation results. Using simulation results variation of carrier's concentrations, valence band edge energy and recombination generation rate for different applied voltage were investigated.

Keyword: Single crystal silicon nanowire; Atomic force microscope nanolithography; Silicon on insulator; KOH wet etching