Analysis and modeling of ASIC area at early-stage design for standard cell library selection

ABSTRACT

Area-delay curve is an effective technique to compare and select the appropriate library at different target delay constraint. However, generating area-delay curve requires time-consuming synthesis processes. This paper presents a fast area estimation model to allow the designer to select the optimal library for designing area-optimized circuit. The model predicts the area-delay curves for a target circuit based on reduced number of synthesis performed at different frequencies. As compared to the general linear search method, the proposed model with 5 synthesis points results 16.5X-18.6X runtime reduction with average error of 2.74%~5.74% in different height libraries implementation. This shows that the proposed model is beneficial for area optimal library selection at the early stage of design.

Keyword: Area estimation; Analysis and modeling; ASIC design; Logic synthesis; Standard cell; Cell height