
**UNIVERSITI PUTRA MALAYSIA**

# *FABRICATION AND SIMULATION OF P-TYPE JUNCTIONLESS SILICON NANOWIRE TRANSISTOR USING SILICON ON INSULATOR AND ATOMIC FORCE MICROSCOPE NANO LITHOGRAPHY*

**ARASH DEHZANGI**

**FS 2012 27**

# FABRICATION AND SIMULATION OF P-TYPE JUNCTIONLESS SILICON NANOWIRE TRANSISTOR USING SILICON ON INSULATOR AND ATOMIC FORCE MICROSCOPE NANO LITHOGRAPHY

**By**

**ARASH DEHZANGI**



**Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Doctor of Philosophy**

**June 2012**

## DEDICATION

**This thesis is dedicated to:**

***My father's soul and my precious mother.***

Abstract of thesis presented to the Senate of Universiti Putra Malaysia, in fulfillment of the Requirement for the degree of Doctor of Philosophy

**FABRICATION AND SIMULATION OF P-TYPE JUNCTIONLESS SILICON NANOWIRE TRANSISTOR USING SILICON ON INSULATOR AND ATOMIC FORCE MICROSCOPE NANO LITHOGRAPHY**

By

**ARASH DEHZANGI**

**June 2012**

**Chairman : Professor Elias Saion, PhD**

**Faculty : Science**

Departing from microelectronic to nanoelectronics, nowadays, is one of the promising and crucial areas in the field of nanotechnology. Relevant difficulties emerge from this scaling down electronic device to nanometres dimension are the fabricating process of nanostructures and understanding the transport mechanism. Scanning tunneling microscope (STM) and atomic force microscope (AFM) commonly used for measuring surface properties of materials at atomic precision, could be manipulated to fabricating nanoscale electronic devices. In this work, AFM nanolithography via local anodic oxidation (LAO) process was used to fabricate side gate Junctionless Silicon Nanowire Transistors (JLSNWTs).

Single element of lightly doped ($10^{15}cm^{-3}$) p-type (100) silicon-on-insulator (SOI) wafer was used to construct the new JLSNWT consisting common transistor components, the source, the drain, and the gate. The novelty for this device is the nanowire, a channel connecting the source and the drain in a single piece without an ohmic contact. Using AFM nanolithography method the nanowire of length 200 nm, width 100 nm, and thickness 90 nm has successfully constructed. To fabricate JLSNWT, a SOI wafer was cut into a chip of 1 cm x 1 cm size, before undergoing cleaning process to remove ionic, heavy metallic or organic contamination desorption. Hydrogen fluoride in 2% water was treated to the wafer surface for 1 minute to replace the Si–O bonds by low energy Si–H bonds and unreceptive the top Si layer to avoid contaminant and native oxide. The lithographic area on SOI for the construction of JLSNWT was about 15 µm x 15 µm and the fabrication process was observed throughout using an optical microscope with the magnification of 100X attached to CCD camera monitor. The anodization of the Si–H surface was performed under negatively biased to the AFM conductive Cr/Pt tip to draw pre-designed nanoscale oxide pattern of the transistor structure. The lithographic area was chemically etching with diluted KOH and isopropanol to remove Si layer outside the pattern and later with diluted hydrogen fluoride to remove oxide ($SiO_2$) on the pattern and finally leaving p-type Si layer on the pattern of JLSNWT. Two JLSNWTs were fabricated and investigated the performance, each having the gap of 75 and 100 nm respectively, between the gate and the channel.

The electrical characteristics of the single lateral gate of JLSNWT were measured by HP4156c semiconductor parameter analyzer at room temperature. The writing speed and applied tip voltage were held at0.5 µm/s and 9 V respectively. The field effect performances in terms of $I_D$-$V_{SD}$ and $I_D$-$V_G$ characteristics were calculated, with subthreshold swing of 170 mV/decade and the ON- OFF ratio of $10^5$. The device works as the Junction-less Transistor (JLT) for negative gate voltage and the pinch-off effect observed in positive voltage. By increasing the gate voltage negatively, the device would bring into accumulation mode which not provide remarkable rising in current value in ON state due to lowest doping concentration. The field effect mobility calculated about 160 $cm^2V^{-1}$ $s^{-1}$ for high electric field.

The $I_D$-$V_{DS}$ simulation shows that the drain current increases and saturated with high and negative voltage of $V_{DS}$ and the p-type JLSNWT device is at ON state. The $I_D$-$V_G$ simulation shows that the drain current increases significantly and saturated by increasing the negative gate voltage, and the device is at ON state. The simulation results for $I_D$ -$V_D$ and $I_D$ -$V_G$ are in good agreement with the experimental results. The current density in the channel is about 2.5 x $10^{-2}$ $Acm^{-2}$. The simulation results of intrinsic properties indicate that the majority carriers concentration (~$10^{16}/cm^3$) with their mobility of 280 $cm^2V^{-1}$ $s^{-1}$ along the nanowire. The minority carriers (~$10^4/cm^3$), the electrons occur on the surface of the channel but not at the source or the drain. These conduction electron share intrinsic properties of nanowire in p-type JLSNWT generated by breaking covalent bonds of bulk Si into Si nanowire.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

**FABRIKASI DAN SIMULASI TRANSISTOR NANOWAYAR SILIKON JENIS-P TANPA SIMPANG DIPERBUAT DARPADA SILIKON ATAS PENEBAT DENGAN KAEDAH NANOLITROGRAFI ATOMIC FORCE MICROSCOPE**

Oleh

**ARASH DEHZANGI**

**Jun 2012**

**Pengerusi : Profesor Elias Saion, PhD**

**Fakulti : Sains**

Beredar dari mikroelektronik kepada nanoelektronik, pada masa kini merupakan salah satu pengharapan penting dalam bidang nanoteknologi. Kesukaran munculnya pengecilan dimensi peranti elektronik sehingga skala nanometer adalah dalam proses fabrikasi struktur-struktur nano dan memahami mekanism pengangkutannya. Imbasan mikroskop terowong (STM) dan mikroskop daya atom (AFM) yang lazim digunakan untuk mengukur sifat-sifat permukaan bahan berketepatan atom, boleh dimanipulasi fungsinya untuk fabrikasi peranti elektronik berskala nano. Dalam penyelidikan ini, nanolitrografi AFM melalui proses pengoksidaan anod tempatan telah digunakan untuk mendapatkan pintu sisi transistor nanowayar silikon tanpa simpang (JLSNWTs).

Wafer elemen tunggal terdop rendah ($10^{15}cm^{-3}$) jenis-p (100) silikon-atas-penebat (SOI) telah digunakan untuk membina JLSNWT baru yang terdiri daripada komponen transistor biasa iaitu Sumber, Parit, dan Pintu. Khas untuk digunakan dengan peranti ini adalah nanowayar, iaitu saluran yang menghubungkan Sumber dan parit daripada bahan tunggal tanpa rintangan. Dengan menggunakan kaedah nanolitrografi AFM nanowayar panjangnya 200 nm, lebar 100 nm, dan ketebalan 90 nm telah berjaya dibina. Untuk fabrikasi JLSNWT, wafer SOI telah dipotong kecil bersaiz 1 cm x 1 cm, sebelum menjalani proses pembersihan untuk mengeluarkan ion, pencemaran logam berat atau organik nyahjerapan. Asid hidrogen florida dalam air telah dirawat ke permukaan wafer selama 1 minit untuk menggantikan ikatan Si-O oleh tenaga rendah ikatan Si-H dan lapisan atas Si yang pasif untuk mengelakkan pencemaran dan oksida tempatan. Kawasan litografi SOI untuk pembinaan JLSNWT adalah kira-kira 15 μm x 15 μm dan proses fabrikasi telah dipantau dengan menggunakan mikroskop optik dengan pembesaran 100X dihubungkan kepada kamera CCD untuk memantau. Penganodan permukaan Si-H telah dilakukan di bawah voltan negatif pada jarum AFM iaitu Cr/Pt untuk melukis terlebih dahulu rekabentuk corak oksida skalanano struktur transistor. Kawasan litografi telah dihapuskan dengan KOH cair dan isopropanol untuk membuang lapisan Si di luar corak rekabentuk dan kemudian dengan hidrogen fluorida cair untuk mengeluarkan oksida ($SiO_2$) pada corak dan akhirnya meninggalkan lapisan Si jenis-p di atas corak JLSNWT. Dua jenis JLSNWTs telah direka dan disiasat prestasi, setiap satu mempunyai jurang pintu masing-masing 75 dan 100 nm, di antara pintu dan nanowayar.

Ciri-ciri elektrik pintu tunggal sisi JLSNWT diukur dengan penganalisa parameter semikonduktor HP4156c pada suhu bilik. Kelajuan tulisan dan voltan jarum telah ditetapkan pada 0.5 μm / s dan 9 V masing-masing. Prestasi kesan bidang ciri-ciri $I_D$-$V_{SD}$ dan $I_D$-$V_G$ telah dikira. Simulasi $I_D$-$V_{DS}$ menunjukkan bahawa arus Parit meningkat dan tepu dengan voltan $V_{DS}$ tinggi dan negatif dan peranti JLSNWT jenis-p berada pada keadaan ON. Simulasi $I_D$-$V_G$ menunjukkan bahawa arus Parit meningkat ketara dan tepu dengan pintu voltan meningkat dan negatif, dimana peranti berada dalam keadaan ON. Keputusan simulasi $I_D$-$V_{DS}$ dan $I_D$-$V_G$ bersetuju baik dengan keputusan eksperimen.Ketumpatan arus dalam saluran adalah kira-kira 2.5 x $10^{-2}$ $Acm^{-2}$. Keputusan simulasi ciri intrinsik menunjukkan bahawa kepekatan majoriti pembawa (~ $10^{16}/cm^3$) dengan pergerakan mereka 280 $cm^2V^{-1}$ $s^{-1}$ sepanjang nanowayar. Pembawa minoriti (~ $10^4/cm^3$), ialah elektron yang terbentuk pada permukaan nanowire tetapi tidak pada Sumber atau Parit. Elektron konduksi ini merupakan ciri intrinsik nanowayar dalam JLSNWT jenis-p dihasilkan dengan memecahkan ikatan kovalen Si pukal kepada Si nanowayar.

## ACKNOWLEDGEMENTS

At the end of this step of my graduate period has allowed for a bit of reflection, and the many people who have contributed to both my work, and my life during of this period of time. First, I would like to express my full appreciation my great dear supervisor, Prof. Dr. Elias Saion for all of guidance, discussions, unlimited assistance consultations and support. I learned from him a lot. He also taught me how to look at the life. I owe him in whole of my life. I also would like to thank my committee members; Prof. Dr. Sabar Derita Hutagalung, Dr. Mohd Nizar B Hamidon and Assoc. Prof. Dr. Jumiah BT Hassan, for their invaluable suggestions, beneficial advices and their endless helps. I would like to give my special thanks to Prof. Dr. Sabar Derita Hutagalung for his encouragement and guidance during my study. I also would like to give my special and pure appreciation of my dear friends and lab mates Mr. Ahmad Makarimi Bin Abdullah and Mr. Farhad Larki for their guidance, support and huge assistance during the project.

I wish to acknowledge my gratitude to all lecturers and staffs in Physics Department of Faculty of Science and also the staff in the electronic lab in school of materials and mineral resources in USM Engineering Faculty for their cooperation. I would like to express my full thanks and sincere gratitude to my dear mother Zahra and my brothers Omid Dehzangi and Iman Dehzangi for their encouragements, emotional supports and fortitude efforts in my life time. I am also grateful to my friends Mr.

Karim Saeedi, Ms. Farzaneh Saadati, Ms. Dr. Bita Basiri, Mr. Ali Sabri and Mrs. Zahra Ajdari for their notice about me and their support during my study.

I also gratefully acknowledge that this work was financially supported by the Science Fund from the Ministry of Science, Technology and Innovation (MOSTI), Malaysia, under project no. **03-01-05-SF0384**, the USM Short Term Grant under project no. **304/PBAHAN/6039035**, and UPM FRGS no. **5524051**.

**ARASH DEHZANGI**
JUNE 2012

I certify that an Examination Committee has met on 1st of June 2012 to conduct the final examination of Arash Dehzangi on his Doctor of Philosophy thesis entitled " **Fabrication and simulation of p-type Junctionless Silicon nanowire transistor Using Silicon On Insulator and Atomic Force Microscope nano lithography"** in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U. (A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.



**BUJANG BIN KIM HUAT,PhD**
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

**Elias Saion, PhD**
Professor
Faculty of Science
Universiti Putra Malaysia
(Chairman)

**Jumiah BT Hassan, PhD**
Assoc. Professor
Faculty of Science
Universiti Putra Malaysia
(Member)

**Mohd Nizar B Hamidon, PhD**
Faculty of Engineering
Universiti Putra Malaysia
(Member)

**Sabar Derita Hutagalung, PhD**
Assoc. Professor
School of Materials and Mineral resources engineering
Universiti Sainc Malaysia (USM)
(Member)

**BUJANG BIN KIM HUAT, PhD**
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date:

## DECLARATION

I declare that the thesis is my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or at any other institution.

**ARASH DEHZANGI**

Date: June 2012

## TABLE OF CONTENT


| | | | Page |
|---|---|---|---|
| **DEDICATION** | | | **ii** |
| **ABSTRACT** | | | **iii** |
| **ABSTRAK** | | | **vi** |
| **ACKNOWLEDGEMENTS** | | | **ix** |
| **APPROVAL** | | | **xi** |
| **DECLARATION** | | | **xiii** |
| **LIST OF TABLES** | | | **xvii** |
| **LIST OF FIGURES** | | | **xviii** |
| **LIST OF ABBREVIATIONS** | | | **xxv** |
| **CHAPTER** | | | |
| **1** | **INTRUDUCTION** | | 1 |
| | 1.1 | Background and motivation | 1 |
| | 1.2 | Problem Statement | 3 |
| | 1.3 | Significant of study | 4 |
| | 1.4 | Objectives of the study | 5 |
| | 1.5 | Outline of the thesis | 5 |
| **2** | **LITERATURE REVIEW** | | 7 |
| | 2.1 | MOSFETs scaling down and barriers | 7 |
| | 2.1.1 | MOSFETs scaling down | 7 |
| | 2.1.2 | Short channel effects (SCEs) | 8 |
| | 2.1.3 | Band to band tunneling and scattering effect | 10 |
| | 2.2 | Silicon nanowire transistor | 11 |
| | 2.2.1 | Bottom-up and top-down fabrication method for SNWTs | 13 |
| | 2.2.2 | Silicon nanowire device and parameters | 17 |
| | 2.3 | Junctionless nanowire transistor | 21 |
| | 2.3.1 | Introduction of junctionless nanowre transistor | 22 |
| | 2.3.2 | Back ground and fabrication method | 23 |
| | 2.3.3 | Characteristic and property of junctionless nanowire transistor | 27 |
| | 2.3.4 | P-type Junctionless silicon nanowire transistor (JLT) | 29 |
| | 2.4 | AFM Nanolithography | 29 |
| | 2.4.1 | Introduction of AFM | 30 |
| | 2.4.2 | AFM overall view and some applications | 31 |
| | 2.4.3 | Force Lithography or Direct Mechanical Modification | 36 |
| | 2.4.4 | Nanofabrication by chemically Modifying Surfaces | 37 |
| | 2.5 | Local Anodic Oxidation (LAO) by AFM | 39 |
| | 2.5.1 | Introduction and background of LAO | 39 |
| | 2.5.2 | Sample preparation for LAO | 40 |
| | 2.5.3 | Oxidation mechanism and process in LAO | 42 |
| | 2.5.4 | AFM-LAO lithography for fabrication of device | 44 |
| **3** | **THEORY** | | 48 |
| | 3.1 | P-type MOS ideal system and electronics | 48 |

3.2 P-type channel MOSFET electronics, parameters and characteristics 50
3.2.1 MOSFET electronics and structure 51
3.2.2 Parameters and characteristics for P-MOSFET 53
3.3 Theory of scaled down MOSFETs 58
3.3.1 Scaled down MOSFETs parameters 59
3.3.2 Saturation current for scaled MOSFETs (Lunstrum's and Natori's theory) 60
3.3.3 Ballistic and quasi-ballistic transport 62
3.4 Junction-less field effect transistor (JLFET) 63
3.4.1 Physics and electrical property of JLFET 64
3.4.2 Short channel effect and effective length 67
3.4.3 Threshold voltage and mobility view 70
3.4.4 I-$V_D$ and I-$V_G$ characteristic of p-type JLFET 72

**4 MATERIALS AND METHODS** 74
4.1 Introduction 74
4.2 Sample preparation 75
4.2.1 Materials and chemicals 75
4.2.2 SOI wafer preparation 76
4.2.3 Sample cleaning process 77
4.3 AFM Local anodic oxidation (LAO) nanolithography 79
4.3.1 AFM instrument 79
4.3.2 Design of the device's structure 82
4.3.3 Procedure delivery 83
4.3.4 Patterning process by AFM-LAO 84
4.3.5 Effective parameter for LAO patterning 88
4.4 Etching processes 89
4.4.1 Introduction 89
4.4.2 KOH etching 89
4.4.3 HF etching and oxide mask removal 91
4.5 Device characterization 92
4.6 Simulation process 95
4.6.1 Introduction 95
4.6.2 Creating structure 96
4.6.3 Meshing the structure 98
4.6.4 Physics of Sentaurus device 99
4.6.5 Solve section and Coupled Command 105
4.6.6 The plug in and Quasi-stationary Command 106
4.6.7 Sentaurus workbench (SWB) 106
4.6.8 Tecplot 107

**5 RESULTS AND DISCUSSION** 109
5.1 Introduction 109
5.2 Contributing parameters in fabrication of JLSNWT 110
5.2.1 Contribution of cleaning and preparation 110
5.2.2 Contribution of applying voltage on the AFM tip and exposure time 113

5.2.3 Contribution of the Relative humidity percentage (RH %) and temperature 115
5.2.4 Effect of KOH etching process on device fabrication 121
5.2.5 Optimum condition for KOH etching 131
5.2.6 Effect of oxide removal on device fabrication 135
5.2.7 Other parameters issues 138
5.3 Characterization of the JLSNWT 142
5.3.1 Introduction 142
5.3.2 Characterization of the device 146
5.3.3 $I_D$-$V_G$ characteristics 147
5.3.4 $I_D$-$V_{SD}$ characteristics 149
5.3.5 Subthreshold slope (SS) 151
5.4 Discussion 152
5.4.1 Accumulation mode junctionless transistor comparison 152
5.4.2 Side gate JLSNWT 153
5.4.3 Mobility view 155
5.4.4 Model description 156
5.5 Numerical simulation of the JLSNWT 166
5.5.1 Introduction 166
5.5.2 The structure creation and parameters 167
5.5.3 Device Simulation Models 168
5.6 Simulation result and discussion 169
5.6.1 $I_D$ - $V_{SD}$ and transfer characteristics 169
5.6.2 Electric field along the nanowire 172
5.6.3 Valence band energy along the nanowire 175
5.6.4 Hole density and electron density along the nanowire 177
5.6.5 OFF state condition 183
5.7 Mobility investigation 186
5.7.1 Band structure and hole transport 186
5.7.2 Mobility improvement due to device configuration 187
5.7.3 Field effect mobility 191
5.7.4 Simulation result 192
5.7.5 Discussion 194

**6 CONCLUSSION** 197
6.1 Conclusion 197
6.2 Suggestion for future work 200

**REFERENCES** **201**
**BIODATA OF STUDENT** **217**
**LIST OF PUBLICATIOS** **218**