Pinch-off effect in p-type double gate and single gate junctionless silicon nanowire transistor fabricated by atomic force microscopy nanolithography

ABSTRACT

The spark of aggressive scaling of transistors was started after the Moors law on prediction of device dimensions. Recently, among the several types of transistors, junctionless transistors were considered as one of the promising alternative for new generation of nanotransistors. In this work, we investigate the pinch-off effect in double gate and single gate junctionless lateral gate transistors. The transistors are fabricated on lightly doped (1015) p-type Silicon-on-insulator wafer by using an atomic force microscopy nanolithography technique. The transistors are normally on state devices and working in depletion mode. The behavior of the devices confirms the normal behavior of the junctionless transistors. The pinch-off effect appears at VG +2.0 V and VG +2.5 V for fabricated double gate and single structure, respectively. On state current is in the order of 10-9 (A) for both structures due to low doping concentration. The single gate and double gate devices exhibit an Ion/Ioff of approximately 105 and 106, respectively.

Keyword: Atomic force microscope; Nanolithography; Junctionless transistor; Pinch off; Nanowire