Simulation of transport in laterally gated junctionless transistors fabricated by local anodization with an atomic force microscope

ABSTRACT

In this paper, we have investigated the characteristics and transport features of junctionless lateral gate transistors via measurement and simulations. The transistor is fabricated using an atomic force microscopy (AFM) nanolithography technique on silicon-on-insulator (SOI) wafer. This work develops our previous examination of the device operation by using 3D numerical simulations to offer a better understanding of the origin of the transistor operation. We compare the experimental measurements and simulation results in the transfer characteristic and drain conductance. We also explore the behavior of the device in on and off states based on the variation of majority and minority carriers' density, electric-field components, and recombination/generation rate of carriers in the active region of the device. We show that the device is a normally on device that can force the current through a depleted region (off state) and uses bulk conduction instead of surface conduction. We also found that due to the lateral gate design, low-doped channel, and lack of the gate oxide the electrostatic squeezing of the channel effectively forces the device into the off state, but the current improvement by accumulation of carriers is not significant.

Keyword: Atomic force microscopy; Junctionless transistors; Nanolithograpy; TCADAD; Technology computer aided design; Simulation