

## Area efficient test circuit for library standard cell qualification

### ABSTRACT

High cost of qualifying library standard cells on silicon wafer limits the number of test circuits on the test chip. This paper proposes a technique to share common load circuits among test circuits to reduce the silicon area. By enabling the load sharing, number of transistors for the common load can be reduced significantly. Results show up to 80% reduction in silicon area due to load area reduction.

**Keyword:** Delay chain; Library validation; On-silicon measurement; Standard cell qualification; TEG circuit