**Design of a testchip for low cost IC testing.**

ABSTRACT

With the continuous increase of the integration densities and complexities, the problem of testing integrated circuits has become much more acute and needs an economic solution with reliable performance. This paper presents the design of a TESTCHIP implementing a multiple polynomial, multiple seed based mixed-mode test technique. Fault simulation experiments on benchmark circuits show that the TESTCHIP is capable of detecting 100% of the faults using a much lower number of test vectors than in the approaches attempted by the other researchers. It also offers lower data storage requirements than that of conventional ATE. The TESTCHIP is capable of testing combinational circuits as well as sequential circuits with scan-path facilities.

**Keyword:** Testchip; IC testing.