ALU CIRCUIT DESIGN MIX LOGIC STYLES TECHNIQUE

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2004

Abstract of this thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

ALU CIRCUIT DESIGN USING MIX LOGIC STYLES TECHNIQUE

By

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Jan 2004

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Arithmetic Logic Unit (ALU) is the heart of microprocessor. It is basically a combinational circuit that performs a number of arithmetic and logic functions. Hence, its performance is crucial for the design of high performance digital computer system.

For the past two decades, Complementary Metal Oxide Semiconductor (CMOS) has been the dominant logic style in digital logic design. Its success is mainly contributed by the low power dissipation, compact design, adequately high speed, simple circuitry and robustness against transistor and voltage scaling properties.

However, the advancement of digital computer technology has requires higher circuit speed. Thus, alternative logic styles need to be found. Complementary Pass-transistor Logic (CPL) proved to be a viable alternative to CMOS logic. Its strength lies in the absence of slow PMOS transistors in the logic path, low input capacitance and higher speed.

A performance comparison had been made between CMOS and CPL logic styles. Logic units and arithmetic units had been designed and compared of their performance in circuit delay, power dissipation and circuit size. Measurement results had showed that CMOS is dominant in simple monotonic logic gates, while CPL performs better for more complex circuit such as multiplexer and arithmetic units. 4-bits ALU is design using full CMOS logic style and also mix logic styles (using the best of both CMOS and CPL). Mix logic styles 4-bits ALU has 76% less power dissipation compared to full CMOS implementation 4-bits ALU. It also has higher speed than full CMOS design but with some marginal increase in circuit size. Hence, mix logic styles has proved to be a viable alternative to full CMOS design for high performance ALU and other digital logic designs.

Abstrak thesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

REKAAN LITAR ALU DENGAN MENGGUNAKAN TEKNIK LOGIC CAMPURAN

Oleh

LEE SENG SIONG

Januari 2004

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Arithmetic Logic Unit (ALU) ialah pusat kepada mikro-pemproses. Secara ringkasnya, ia adalah kombinasi litar yang dapat menjalankan fungsi-fungsi arimetik dan logik. Oleh sebab itu, kemampuannya adalah sangat penting di dalam rekaan sistem komputer digital yang berkemampuan tinggi.

Sejak dua dekad yang lepas, Complementary Metal Oxide Semiconductor (CMOS) adalah jenis logik yang dominan dalam rekaan logik digital. Kejayaannya adalah disebabkan oleh ciri-cirinya yang berpengunaan kuasa rendah, rekaan yang mampat, berkelajuan yang agak tinggi, dan stabil untuk penskalaan transistor dan voltan.

Akan tetapi, kelajuan yang lebih tinggi amatlah diperlukan dengan kemajuan yang pesat dalam bidang pemkomputeran digital. Oleh sebab itu, kaedah logik alternatif hendaklah dikenal pasti. Complementary Pass-transistor Logic (CPL) adalah calon alternatif yang

sesuai untuk menggantikan CMOS. Kelebihannya adalah kerana ketiadaan transitor PMOS yang lambat, kapasitan input yang rendah serta berkelajuan tinggi.

Satu perbandingan dari segi kemampuan telah dijalankan antara CMOS dan CPL. Unit-unit logik dan arimetik telah direka dan dibandingkan dari segi kemampuannya dalam kelajuan litar, pengunaan kuasa, dan saiz litar. Keputusan ukuran telah menunjukkan bahawa CMOS adalah lebih dominan dalam get litar ringkas yang "monotonic", tetapi CPL lebih berkemampuan dalam litar yang lebih kompleks, seperti multiplexer dan litar-penambah penuh. ALU 4-bit telah direka dengan menggunakan kaedah logik CMOS dan kaedah logik campuran (menggunakan unit yang terbaik dari logic CMOS dan CPL). ALU 4-bit logic campuran menunjukkan 76% penjimatan dalam penggunaan kuasa jika dibandingkan dengan ALU 4-bit CMOS. Ia juga mempunyai kelajuan yang tinggi tetapi dengan sedikit pengingkatan dalam saiz litar. Oleh sebab itu, kaedah logik campuran telah terbukti sebagai kaedah alternative yang sesuai berbanding CMOS dalam perekaan ALU serta lain-lain litar logik digital yang berkemampuan tinggi.

ACKNOWLEDGEMENTS

I would like to thank GOD for the blessings that He had showered into my life. For providing me the wisdom needed to pursue the knowledge of the universe.

I want to express my greatest gratitude to En. Rahman Wagiran, my project chairman for his patient, support and invaluable guidance during the course of the project research.

Special thanks also to Dr. Roslina Sidek, En. Nasri Sulaiman and En. Wan Zuha for their advice, guidance, attention and help.

Last but not least, I would like to thank my family and friends for their patience and moral support.

I certify that an Examination Committee has met on…12th January, 2004…to conduct the final examination of Lee Seng Siong on his Master of Science thesis entitle "ALU Circuit Design Using Mix Logic Styles Technique" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulation 1981. The Committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows :

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DECLARATION

I hereby declare that the thesis is based on my original work except for the quotations and citations which have been duly acknowledge. I also declare that it has not been previously or concurrently submitted for any degree at UPM or other institutions.

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LEE SENG SIONG

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