

Optimality of bus-invert coding

ABSTRACT

Dynamic power dissipation on I/O buses is an important issue for high-speed communication between chips. One can use coding techniques to reduce the number of transitions, which will reduce the dynamic power. Bus-invert coding is one popular technique for interchip buses, where the dominant contribution is from the self-capacitance of the wires. This algorithm uses an invert line to signal whether the bus data are in its original or an inverted form. While the method appears to be a greedy algorithm, we show that it is, in fact, an optimal strategy. To do so, we first represent the bus and invert line using a trellis diagram. Then, we show that applying bus-invert coding to a sequence of words gives the same result as would be obtained by using the Viterbi algorithm, which is known to be optimal. We also show that partitioning an M -bit bus into P subbuses and using bus-invert coding on each subbus can be described as applying the Viterbi algorithm on a 2^P -state trellis.

Keyword: Bus coding; Low power; Off-chip buses; Trellis diagram; Viterbi decoding.