

Article

A PVT-Robust 0.8 V Subthreshold Double-Tail Dynamic Comparator with 20.7 fJ/Comparison-Step Energy Efficiency for 10-Bit SAR ADCs

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Abstract

Dynamic comparators are key building blocks in low-power successive-approximation-register (SAR) analog-to-digital converters (ADCs), where energy efficiency, decision speed, and reliable operation under process, voltage, and temperature (PVT) variations are essential design requirements. This paper presents a 0.8 V subthreshold double-tail dynamic comparator incorporating a threshold-controlled latch activation mechanism for differential 10-bit SAR ADC applications. By delaying latch regeneration until sufficient differential voltage amplification is established by the dynamic amplifier stage, the proposed architecture suppresses premature regeneration, reduces kickback-induced disturbances, and improves comparator operation under low-voltage conditions. To comprehensively evaluate robustness under extreme operating conditions, a dedicated Input Test Pattern (ITP)-based validation methodology was developed and applied across 45 PVT corners comprising TT, SS, FF, FS, and SF process conditions, $\pm 10\%$ supply-voltage variation (0.72–0.88 V), and temperatures ranging from 0 °C to 100 °C. The comparator was implemented in a 180 nm CMOS technology and evaluated through schematic and post-layout simulations. Under nominal operating conditions, the proposed comparator resolved a minimum differential input voltage of 0.8 mV while achieving a post-layout regeneration delay of 327 ps, an average power consumption of 41.4 nW, and an energy efficiency of 20.7 fJ/comparison-step. In addition, the proposed architecture achieved a peak-to-peak kickback noise of 197 mV and successfully passed all 45 post-layout PVT corner simulations, demonstrating reliable functionality under wide process, voltage, and temperature variations. These results validate the effectiveness of the proposed threshold-controlled latch activation mechanism and the ITP-based validation methodology, demonstrating that the proposed JRR2 comparator provides an effective balance among low-voltage operation, decision speed, ultra-low-power consumption, energy efficiency, and robustness for differential 10-bit SAR ADC applications.

Keywords: dynamic comparator; double-tail comparator; SAR ADC; process–voltage–temperature variation; metastability; energy-efficient circuits



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1. Introduction

The growing emphasis on low-power and sustainable energy solutions highlights the essential need for ultra-low-power circuit designs in modern electronics. This demand is especially relevant for system-on-chip (SoC) and Internet-of-Things (IoT) applications, such as self-powered and battery-operated micro-sensor networks, portable medical devices, and wearable technology [1–3]. In these contexts, energy efficiency is prioritized over speed to maximize battery life and minimize the frequency of replacements. ADCs are crucial in these applications, as they convert analog sensor signals into digital data for further processing.

To minimize power consumption, various strategies focus on optimizing the supply voltage (V_{DD}). Operating at near-threshold levels effectively decreases dynamic energy consumption, given that dynamic power is proportional to the square of V_{DD} [4,5]. However, this approach presents significant challenges for analog circuits, such as comparators, where functioning at subthreshold levels can negatively affect accuracy and speed due to limited voltage headroom [6,7]. While subthreshold designs can achieve remarkably low power consumption and extended operational lifetimes, they also introduce unique challenges that necessitate innovative design techniques and comprehensive testing. Subthreshold circuits are particularly sensitive to variations in PVT; even minor changes in gate-source voltage (V_{GS}) can lead to substantial fluctuations in drain current (I_{DS}), requiring precise control in circuit design [8]. A SAR ADC, consisting of the comparator, SAR logic, and Digital-to-Analog Converter (DAC), benefits from technology scaling to lower the power consumption of the SAR logic. However, optimizing power consumption in the comparator and DAC require advanced design methodologies [9].

A significant challenge in comparator design is metastability, which can severely impact the performance of SAR ADCs [10]. Metastability occurs when the output of the comparator fails to stabilize within the required timeframe, particularly with small differential input signals, potentially leading to inaccuracies, as illustrated in Figure 1. Since SAR ADCs operate in a serial flow, such errors can propagate through the conversion process, affecting overall accuracy [11]. Despite various proposed solutions, many are not practical for low-voltage applications due to limitations associated with analog components, where small signal differences and fabrication variations exacerbate metastability issues [7,9].

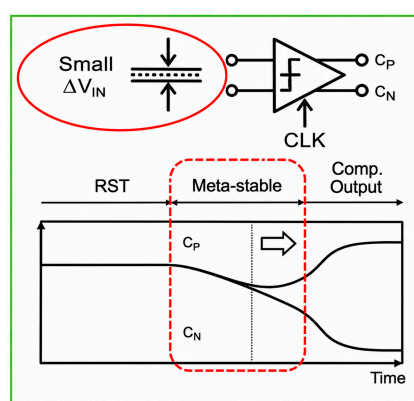


Figure 1. Metastability error in a differential output dynamic comparator with a small differential input voltage.

Double-tail dynamic comparators represent a promising alternative, offering a balance between low power consumption and high-speed operation by incorporating separate amplification and latching stages [5,12]. However, these comparators face challenges such as high-power consumption and kickback noise, particularly at low supply voltages where precision is crucial [2,12–15]. Research has primarily focused on dynamic comparators

under nominal conditions, with limited exploration into how PVT variations affect the performance of low-voltage comparators in SAR ADCs. PVT corner simulations are essential for assessing circuit robustness under extreme variations in transistor properties, supply voltages, and temperatures [16–19]. These variations can significantly impact comparator accuracy and worsen metastability errors, particularly in low-voltage environments [20–23]. To address these challenges, this research validates the performance of double-tail dynamic comparators across 45 PVT conditions using 180 nm CMOS technology, with a 60% reduction in the standard supply voltage. A dedicated Input Test Pattern (ITP) methodology was developed to rigorously assess the design’s robustness, leading to the development of a threshold-controlled double-tail dynamic comparator optimized for energy efficiency, delay performance, and robustness under PVT variations. This work advances the development of reliable, energy-efficient comparators for low-voltage, self-powered devices, ensuring enhanced accuracy and performance in demanding conditions.

Although conventional double-tail dynamic comparators provide an attractive trade-off between speed and power consumption, maintaining reliable operation under low-voltage conditions remains challenging. The Schinkel comparator [13] employs direct latch regeneration following the amplification phase, which can increase sensitivity to process-induced variations and metastability when operating in the subthreshold region. The Paik comparator [16] enhances low-voltage performance through a pseudo-dynamic architecture; however, latch regeneration may still be initiated before adequate differential voltage amplification is established, potentially increasing susceptibility to kickback-induced disturbances and performance degradation under unfavorable PVT conditions. These limitations motivated the development of the proposed JRR2 comparator, which incorporates a threshold-controlled latch activation mechanism that postpones regeneration until sufficient differential voltage amplification is achieved. This approach improves decision robustness, enhances robustness against PVT variations, and reduces unnecessary regenerative activity, resulting in improved energy efficiency under low-voltage operation.

Contribution of This Work

The main contributions of this work are summarized as follows:

- I. A PVT-robust subthreshold double-tail dynamic comparator architecture operating at a 0.8 V supply voltage is proposed for low-power 10-bit SAR ADC applications.
- II. A threshold-controlled latch activation mechanism is introduced through transistors M11 and M12 embedded within the regenerative latch. The proposed mechanism delays latch regeneration until sufficient differential voltage amplification is established by the dynamic amplifier stage, thereby suppressing premature regeneration, reducing kickback-induced disturbances, and improving robustness under low-voltage operation.
- III. A systematic Input Test Pattern (ITP) generation algorithm is proposed to generate critical differential input transition sequences for dynamic comparator validation. The generated ITP sequences facilitate the detection of metastability-prone operating conditions and PVT-dependent failure mechanisms that may not be revealed through conventional fixed-input verification approaches.
- IV. A comprehensive validation framework combining the proposed ITP scheme and 45-corner schematic and post-layout PVT analysis is established to evaluate comparator robustness under PVT variations, including TT, SS, FF, FS, and SF process conditions, $\pm 10\%$ supply-voltage variation, and temperatures ranging from 0 °C to 100 °C.
- V. The proposed JRR2 comparator maintains reliable operation across all 45 PVT corners while achieving a nominal average power consumption of 41.4 nW, an energy

efficiency of 20.7 fJ/comparison-step, and a worst-case post-layout regeneration delay of 105 ns.

- VI. Comparative assessment against representative low-voltage dynamic comparator architecture demonstrates that the proposed design achieves an improved balance between speed, energy efficiency, and robustness.

2. Design Methodology

To reduce power consumption in dynamic comparators, a subthreshold double-tail dynamic comparator operating at a supply voltage of 0.8 V was developed using 180 nm CMOS technology. The design is based on conventional double-tail architecture and incorporates pMOS differential input transistors to improve noise immunity and robustness under low-voltage operation. This design choice helps mitigate inadequate overdrive conditions commonly associated with nMOS input devices when the gate-source voltage (V_{GS}) approaches the threshold voltage (V_{TH}), thereby improving metastability tolerance and overall comparator performance [18].

The comparator was implemented in Cadence Virtuoso and optimized for a 10-bit differential SAR ADC application. For the targeted 10-bit differential SAR ADC, the differential full-scale input range is defined as 1.6 V. Therefore, the comparator must resolve a minimum voltage corresponding to the least significant bit (LSB) generated by the DAC during the successive approximation process. The LSB is calculated as:

$$\text{LSB} = \frac{V_{in}}{\text{Resolution}} = \frac{1.6 \text{ V}}{2^{10}} = 1.56 \text{ mV}$$

To ensure reliable operation during the final SAR conversion cycle, the comparator is designed to resolve at least $\frac{1}{2}$ LSB, corresponding to approximately 0.8 mV. Accordingly, the differential input voltage range (ΔV_{in}) considered in this work spans from 0.8 mV to 800 mV. For a target SAR ADC sampling rate of 200 kS/s, one ADC conversion is completed within approximately 5 μ s. The comparator operates with a 2 MHz evaluation clock during the successive approximation process, corresponding to a clock period of 500 ns. In addition to the comparator decision cycles, the complete conversion sequence includes sampling and SAR control operations. Based on these design requirements, the architectures of two existing dynamic comparators, namely Shin and Paik, are first analyzed to identify their limitations under low-voltage operation. Subsequently, two optimized comparator architectures, referred to as JRR1 and JRR2, are developed and evaluated. The optimum speed of the comparator is characterized by the regeneration delay (t_{delay}), which serves as the primary timing metric throughout the comparative analysis.

2.1. JRR Dynamic Comparator Architecture

The JRR1 comparator is derived from a pseudo-dynamic comparator topology inspired by the Paik comparator [16] to improve stability under low-voltage operation. The primary objective is to reduce power consumption, suppress kickback noise, and improve delay performance relative to the original Paik architecture. Figure 2 illustrates the modifications introduced in the latch stage, including the removal of reset transistors M15 and M16. These transistors were originally incorporated to alleviate hysteresis and improve common-mode voltage (V_{CM}) oscillation near V_{DD} ; however, under a 0.8 V supply voltage and a SAR ADC common-mode voltage of 0.4 V, their impact on kickback noise reduction was found to be negligible. Consequently, M15 and M16 were removed to reduce parasitic capacitance at nodes fP1 and fM1, thereby improving current mobility, shortening regeneration time, and reducing power consumption. To compensate for the resulting reduction in node capacitance, transistors M13 and M14 were introduced as paired tail devices in the latch stage.

These transistors increase effective transconductance (g_m) and enhance latch regeneration performance. The differential dynamic amplifier stage processes the input differential signal before transferring it to the regenerative latch stage. All transistors, except M1/M2 and M13/M14, are sized at $W/L = 1 \mu\text{m}/180 \text{ nm}$. The input transistors M1/M2 are sized at $8 \mu\text{m}/360 \text{ nm}$ to improve input sensitivity and maintain decision accuracy above $\frac{1}{2}$ LSB under PVT variations, while M13/M14 are sized at $1 \mu\text{m}/360 \text{ nm}$ to improve latch regeneration speed.

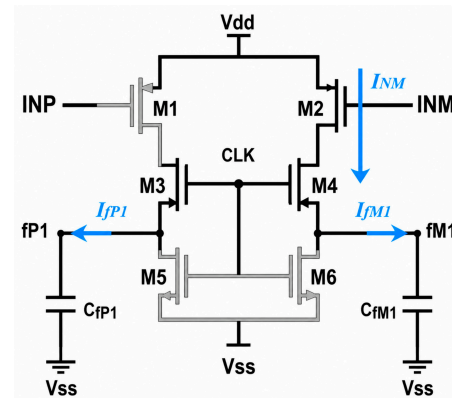


Figure 2. Operation of JRR1 dynamic amplifier circuit during regeneration phase when $V_{\text{INM}} < V_{\text{INP}}$.

For the targeted SAR ADC operating at 200 kS/s, one conversion is completed within approximately 5 μs , while each comparator evaluation cycle is allocated approximately 500 ns, so the comparator is designed to complete comparisons within 500 ns per clock cycle while minimizing power consumption. Figure 2 illustrates the operation of the dynamic amplifier circuit during the regeneration phase. When the CLK signal drops to 0 V, PMOS transistors M3 and M4 turn ON, and M5 and M6 turn OFF, causing output of the dynamic amplifier voltages (V_{fM1} and V_{fP1}) to approximate the input voltages at M1 and M2. When V_{INP} is set to 800 mV and V_{INM} to 0 V, the PMOS input transistor M2 operates in the saturation region while M1 is in the cutoff region. The drain current I_{NM} flows at a rate of $[I_{\text{fM1}}/C_{\text{fM1}}]$, charging the load capacitor C_{fM1} , which represents the input load to the latch stage. Consequently, V_{fM1} approaches V_{DD} while V_{fP1} remains near V_{DSM3} . This differential voltage gain (ΔV_{fMP1}) represents the dynamic amplifier stage's gain:

$$\Delta V_{\text{fMP1}} = V_{\text{fP1}} - V_{\text{fM1}} \quad (1)$$

The schematic diagram in Figure 3 illustrates the operation of the latch circuit during the Regeneration time when $V_{\text{INM}} = 0 \text{ V}$ and $V_{\text{INP}} = 800 \text{ mV}$. At time 1.5 μs , the CLK signal changes to 0 V with a drop time of 1 ps because I_{fM1} on the dynamic amplifier starts to flow to node fM1 with $V_{\text{fM1}} = V_{\text{DSM2}} + V_{\text{DSM4}} \approx V_{\text{DD}}$ and enables the tail of M14. M12 turns ON when M7 is turned ON with $V_{\text{fP1}} = V_{\text{DSM3}} < V_{\text{THM7}}$ at node fP1. Then the differential output voltage $V_{\text{OUTP_JRR1}} = V_{\text{DSM7}} = V_{\text{DD}}$ and $V_{\text{OUTM_JRR1}} \approx 0 \text{ V}$. Terminal OUTP_JRR1 will generate output 0.8 V and terminal OUTM_JRR1 will generate output 0 V.

The JRR2 comparator was developed to further reduce kickback-induced disturbances observed in the JRR1 architecture, particularly affecting the M11 and M12 transistors in the latch stage, which can increase delay and power consumption. Enhancements in the latching and dynamic amplifier stages are implemented similarly to those in the JRR1 comparator. The architecture of the JRR2 comparator is shown in Figure 4. In this design, the differential dynamic amplifier outputs (fP2 & fM2) are connected to NMOS transistors M11 and M12, which are embedded within the back-to-back inverter of the latch stage. This configuration ensures that current flow begins only after sufficient differential voltage

amplification has been established from the dynamic amplifier, thereby reducing kickback noise in the latch stage. Transistors M11 and M12 function both as reset transistors and as tail currents for the latch circuit, minimizing kickback noise during both the regeneration and reset phases. During operation, the dynamic amplifier's output voltages (V_{fP2}/V_{fM2}) initially remain at GND, keeping M11 and M12 OFF and preventing the latch stage from starting the comparison until the common-mode voltage exceeds the NMOS threshold. As illustrated in Figure 5, during the regeneration phase, if the input INP is at 0 V and INM is at 800 mV, a transition of the CLK signal to GND causes the current I_{fP2} to flow to the latch stage at node fP2, turning ON transistor M11 while M8 remains OFF. This process develops sufficient differential voltage gain (ΔV_{fMP2}) at the latch input, ensuring effective performance in the regeneration phase.

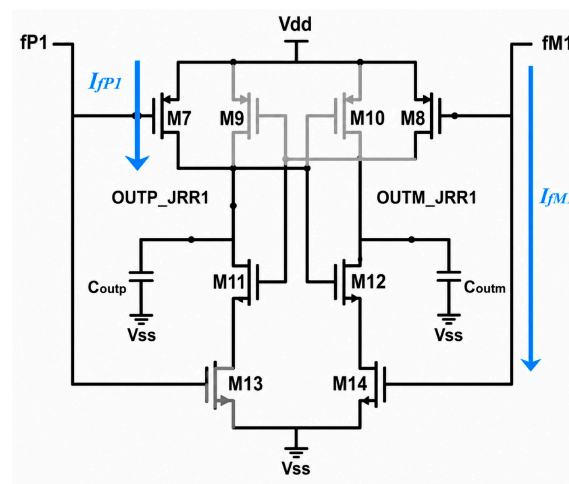


Figure 3. Operation of JRR1 latching circuit during regeneration phase when $V_{INM} < V_{INP}$.

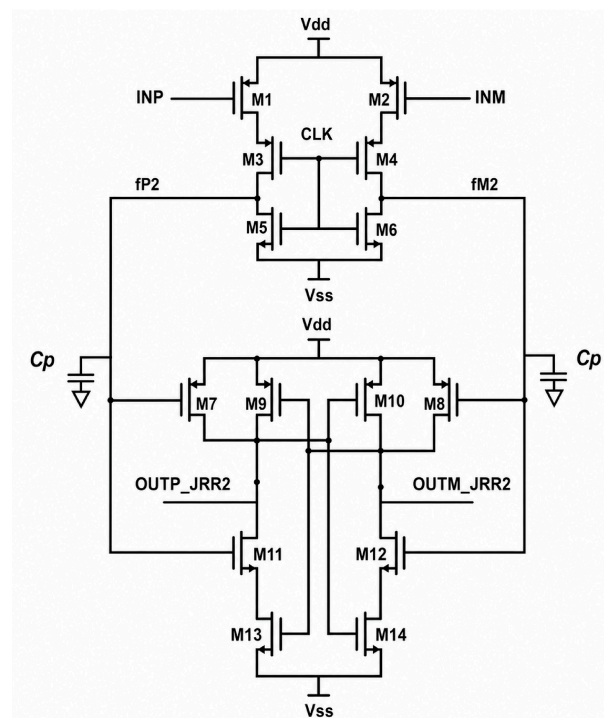


Figure 4. Architecture of proposed JRR2 comparator circuit.

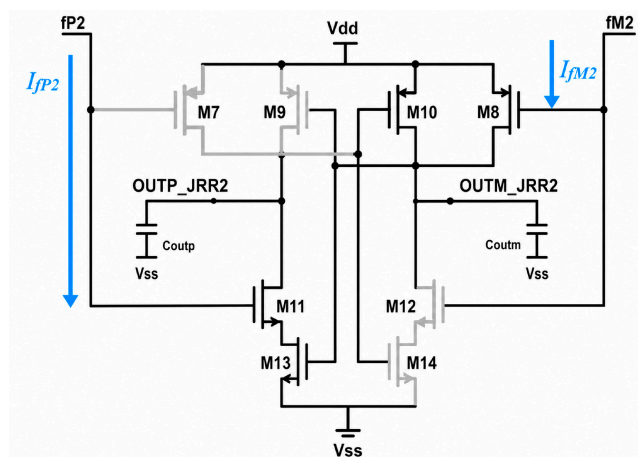


Figure 5. Operation of JRR2 latching circuit during regeneration phase when $V_{INP} < V_{INM}$.

Figure 5 also demonstrates that M11 and M12 ensure the latch stage only begins to compare when the dynamic amplifier's outputs (V_{fP2} & V_{fM2}) rise above the NMOS threshold voltage of M11. When the input INP is set to 0 V and INM to 800 mV, and the CLK signal switches to GND, the I_{fP2} current flows to node fP2, turning ON M11 while M8 remains OFF. As a result, a sufficient ΔV_{fMP2} differential voltage gain is developed at the latch input. At the latch output, OUTP_JRR2 equals $V_{DSM11} + V_{DSM13}$, which is approximately 0, resulting in $C_{outp} = 0$ V. Simultaneously, $V_{GSM10} = 0$ V turns ON M10, making OUTM_JRR2 approximately equal to V_{DD} . Consequently, when the latch stage starts comparing, it experiences an adequate differential voltage gain at its input, enabling reliable regeneration operation.

The key distinction between the proposed JRR2 comparator and conventional double-tail architecture lies in the threshold-controlled activation of the regenerative latch. In the proposed design, transistors M11 and M12 remain OFF until sufficient differential voltage gain is developed by the dynamic amplifier stage. Consequently, latch regeneration is delayed until the input differential signal reaches a level that ensures reliable regeneration. This mechanism suppresses premature regeneration, reduces kickback-induced disturbances, and improves robustness under low-voltage and PVT-varying conditions.

2.2. Novelty and Operating Principle of the Proposed JRR2 Comparator

The novelty of the proposed JRR2 comparator lies in the introduction of a threshold-controlled latch activation mechanism through transistors M11 and M12 embedded within the regenerative latch stage. Unlike conventional double-tail dynamic comparators, where latch regeneration starts immediately after the clock transition, the proposed architecture delays the regeneration process until sufficient differential voltage gain has been established by the dynamic amplifier stage. During the initial amplification period, transistors M11 and M12 remain OFF while the dynamic amplifier develops the differential voltage at nodes fP2 and fM2. As a result, the regenerative latch is temporarily isolated from the amplifier stage, preventing premature regeneration and minimizing kickback-induced disturbances. Once the differential voltage exceeds the threshold voltage of M11 and M12, the latch stage is activated, and regeneration proceeds with a larger initial differential voltage.

Since latch regeneration delay is strongly dependent on the initial differential voltage developed at the latch input, increasing the initial differential voltage improves regeneration efficiency and reduces metastability probability. Consequently, the proposed architecture achieves improved delay performance and enhanced robustness under PVT variations. Furthermore, the temporary isolation between the dynamic amplifier and regenerative latch reduces charge injection from the latch stage to the input nodes, thereby suppressing

kickback noise without introducing additional calibration circuits, auxiliary amplifiers, or compensation networks. These features enable robust operation under low-voltage sub-threshold conditions while maintaining low power consumption and high energy efficiency. Unlike conventional double-tail comparators, the proposed threshold-controlled latch activation mechanism improves regeneration robustness without introducing auxiliary amplifiers, calibration circuits, or additional power overhead.

3. PVT Validation Methodology

The PVT validation methodology for the proposed comparator design involves several key steps. As illustrated in Figure 6, the process begins by defining the validation parameters, which include specifying PVT corner parameters, a 10% variation in V_{DD} , and a specified temperature range. Using the Corners Setup Tool in the simulation environment, 45 PVT corners are configured to create a comprehensive test setup. Next, an ITP scheme is developed to validate the design's performance under worst-case conditions. This involves identifying the worst-case input differential (ΔV_{in}) based on the design specifications and formulating a comprehensive input test sequence that covers all possible scenarios. The corresponding ITP waveform is then generated for use in the simulations.

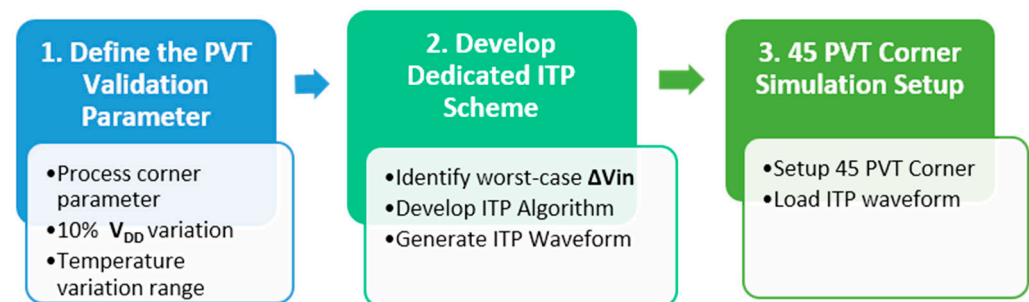


Figure 6. PVT Validation Methodology Flow.

Finally, the 45 PVT corner configurations are set up in the EDA simulator tool, and the ITP waveform is loaded as the differential input voltage for the comparator. The gate voltage of the differential input transistors is configured to respond to the ITP waveform, ensuring that the comparator is thoroughly tested under various PVT conditions. By following this systematic approach, the comparator design can be rigorously tested for robustness and performance across a range of operating scenarios. The ITP scheme plays a crucial role in identifying and validating the design's behavior under worst-case input transitions, which are highly sensitive to PVT variations.

3.1. PVT Validation Parameter

In the context of integrated circuit fabrication, process corners serve as a critical tool for understanding the impact of manufacturing variations on circuit performance. Front-End-of-Line (FEOL) corners have a significant influence on transistor behavior and are commonly denoted using two-letter codes that represent the characteristics of both NMOS and PMOS devices. The “F” (fast) designation indicates high-mobility transistors, which exhibit enhanced speed and power consumption characteristics, while the “S” (slow) designation corresponds to lower-mobility transistors that exhibit reduced speed and power consumption. For PVT validation, parameters based on 10% variation are employed to assess the robustness and performance of the design under consideration.

As outlined in Table 1, the specific process corners selected for validation include a range of fabrication conditions, such as FS, SS, SF, TT, and FF, as defined by the BSIM 180 nm process design kit (PDK). By incorporating these process corners into the validation

methodology, the design can be thoroughly evaluated for its resilience and functionality across a variety of manufacturing scenarios. Table 2 provides the voltage supply and temperature variations applied during validation. The V_{DD} varies by 10% around the nominal value of 0.8 V, ranging from 720 mV to 880 mV, while temperature is tested at three levels: a minimum of 0 °C, a nominal 30 °C, and a maximum of 100 °C.

Table 1. Process Corner Parameter.

Corner Parameter	Condition	
	NMOS	PMOS
<i>FF</i>	FAST—high mobility	FAST—high mobility
<i>SS</i>	SLOW—low mobility	SLOW—low mobility
<i>TT</i>	TYPICAL—nominal	TYPICAL—nominal
<i>FS</i>	FAST—high mobility	SLOW—low mobility
<i>SF</i>	SLOW—low mobility	FAST—high mobility

Table 2. Voltage and Temperature Corner Parameter.

Parameter	Process		
	Min	Typical	Max
Supply Voltage (V)	0.72	0.8	0.88
Temperature (°C)	0	30	100

3.2. Proposed Input Test Pattern (ITP) Scheme

A dedicated ITP-based validation methodology has been developed to evaluate comparator robustness during worst-case ΔV_{in} transitions. This procedure organizes ΔV_{in} across all possible input sequences in SAR ADC operation and incorporates a 45-corner PVT validation setup, with the ITP specifically defined to satisfy the circuit configuration requirements. The development of the ITP scheme is based on the design specifications of the proposed dynamic comparator, which is required to operate with a minimum input differential voltage of 0.8 mV at a supply voltage of 0.8 V and a clock frequency of 2 MHz using 180 nm CMOS technology. The ITP consists of a set of input signal assignments that ensure the circuit operates under specified conditions.

An ITP algorithm has been developed to validate critical input transitions under worse-case differential voltage conditions during PVT simulations. Figure 7 illustrates the state diagram of the proposed ITP algorithm, showing the complete sequence of transitions evaluated under worst-case conditions. To ensure comprehensive coverage, the ITP scenarios include Big Negative (BN), Big Positive (BP), Small Negative (SN), and Small Positive (SP). For example, Big Positive (BP) represents a large positive differential voltage at INP, whereas Small Negative (SN) represents a small negative differential voltage at INM. The numbered arrows (1–12) in Figure 7 indicate the critical input transition sequences evaluated during the ITP validation process, while the different arrow colors distinguish transitions originating from BN, BP, SN, and SP states. This systematic approach ensures that the dynamic comparator is thoroughly tested under a wide range of input conditions, thereby enhancing its robustness and reliability for practical applications.

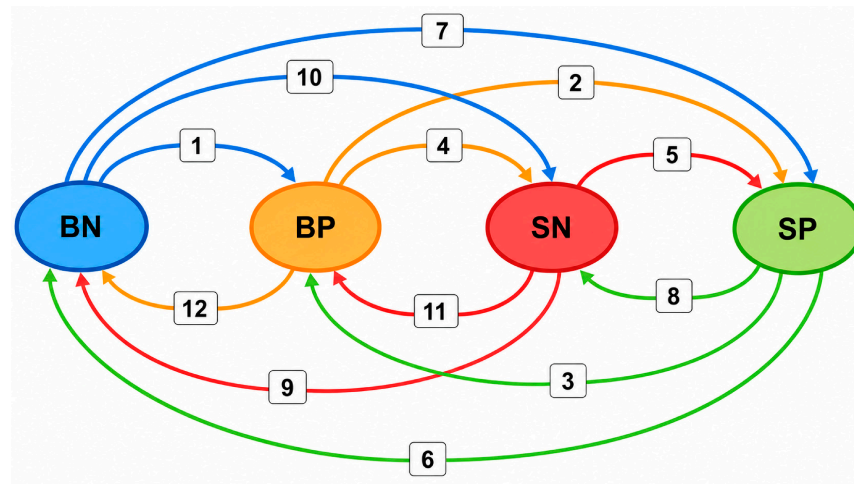


Figure 7. State diagram of the proposed ITP algorithm showing critical input transitions among BN, BP, SN, and SP states.

For this design, a clock frequency of 2 MHz is employed, with each test sequence lasting 1 μ s. The performance assessment involves configuring the input voltages (INP and INM) of the transistors to represent worst-case scenarios: a small ΔV_{in} of 0.8 mV and a large ΔV_{in} of 800 mV, determined based on $\frac{1}{2}$ LSB of a 10-bit digital output. For the small ΔV_{in} , INP is set to 400.4 mV and INM to 399.6 mV, while for the large ΔV_{in} , INP is 800 mV (maximum voltage for logic '1'), and the logic '0' voltage is set to 0 V. The input signals are toggled sequentially from a large positive differential to a small negative, followed by a small positive and then a large negative differential. This sequence ensures that the comparator is tested under various input conditions, including transitions between large and small voltage differences. The test sequence for all possible input differences is systematically organized in Table 3, providing a comprehensive overview of the input configurations used in the PVT corner simulations. This structured approach allows for thorough testing of the comparator's performance under different input scenarios, enabling the identification of potential weaknesses or vulnerabilities in the design.

Table 3. Input Test Pattern sequence.

Test Seq.	Period (μ s)	Input		ΔV_{in} (mV)	Remarks
		INM (mV)	INP (mV)		
1	0–1	800.0	000.0	−800	Big Negative (BN)
2	1–2	000.0	800.0	+800	Big Positive (BP)
3	2–3	399.6	400.4	+0.8	Small Positive (SP)
4	3–4	000.0	800.0	+800	Big Positive (BP)
5	4–5	400.4	399.6	−0.8	Small Negative (SN)
6	5–6	399.6	400.4	+0.8	Small Positive (SP)
7	6–7	800.0	000.0	−800	Big Negative (BN)
8	7–8	399.6	400.4	+0.8	Small Positive (SP)
9	8–9	400.4	399.6	−0.8	Small Negative (SN)
10	9–10	800.0	000.0	−800	Big Negative (BN)
11	10–11	400.4	399.6	−0.8	Small Negative (SN)
12	11–12	000.0	800.0	+800	Big Positive (BP)
13	12–13	800.0	000.0	−800	Big Negative (BN)

By employing a 2 MHz clock frequency and defining the input voltages based on the design specifications, the PVT corner simulations can accurately assess the comparator's behavior under realistic operating conditions. The systematic organization of the test sequences in Table 3 ensures that the design is thoroughly evaluated, contributing to the overall reliability and robustness of the proposed comparator circuit. The test sequence outlined in Table 3 is specifically designed to capture worst-case input transitions that are highly sensitive to PVT variations. By incorporating these critical transitions, the sequence establishes a comprehensive framework for evaluating the dynamic comparator across a range of operating conditions. It encompasses all possible scenarios that may arise during SAR ADC operation, facilitating an in-depth analysis of the comparator's performance and resilience under challenging conditions.

The proposed ITP scheme is derived from a systematic ITP generation algorithm that produces critical differential transition sequences for dynamic comparator validation. By targeting transitions between large and near-zero differential input conditions, the generated test patterns improve the detection of metastability-prone operating conditions and PVT-sensitive failure mechanisms that may not be revealed through conventional fixed-input verification approaches.

These input patterns are subsequently translated into the waveform depicted in Figure 8, which spans a total duration of 13 μs . This waveform visually represents the various input transitions, allowing for a clear understanding of how the comparator responds to different voltage differentials over time. By thoroughly testing these scenarios, the design can be rigorously assessed for its reliability and effectiveness in real-world applications, ensuring that it meets the necessary performance standards under varying conditions.

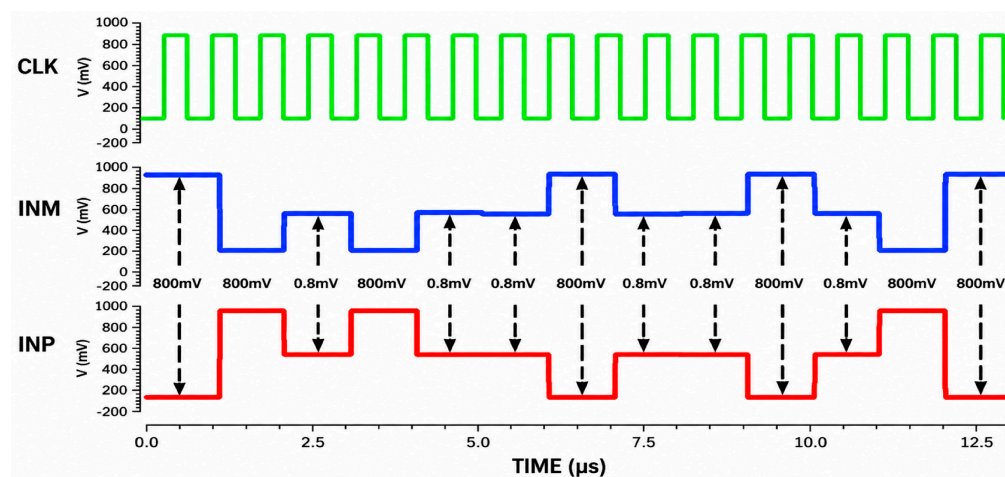


Figure 8. Waveforms generated from Input Test Pattern (ITP) Algorithm.

4. Results and Discussion

To validate the proposed PVT validation methodology, four dynamic comparators (Shin, Paik, JRR1, and JRR2) were simulated under 45 PVT corners. To compare the performance of all comparators, all transistor sizes are scaled to the same dimensions [24,25]. The analysis encompasses delay and power consumption metrics for both schematic and post-layout designs.

4.1. PVT Schematic Simulation

The performance of the proposed comparator circuit under PVT variations is evaluated through schematic simulations. The results from the PVT corner simulations of the JRR2 comparator circuits are displayed on Figure 9. The JRR2 comparator operates correctly under the 45 PVT corner conditions, demonstrating a differential input voltage (ΔV_{in}) of

0.8 mV at $V_{DD} = 0.8$ V and a clock sampling rate of 200 kS/s. The findings indicate that the JRR2, JRR1, and Paik comparators function accurately across the 45 PVT corner test setups. In contrast, the Shin comparator circuit schematic encountered failures at specific PVT corners, as illustrated in Figure 10. This analysis highlights the robustness of the JRR2 comparator while identifying vulnerabilities in the Shin comparator under varying conditions, emphasizing the importance of thorough testing in circuit design.

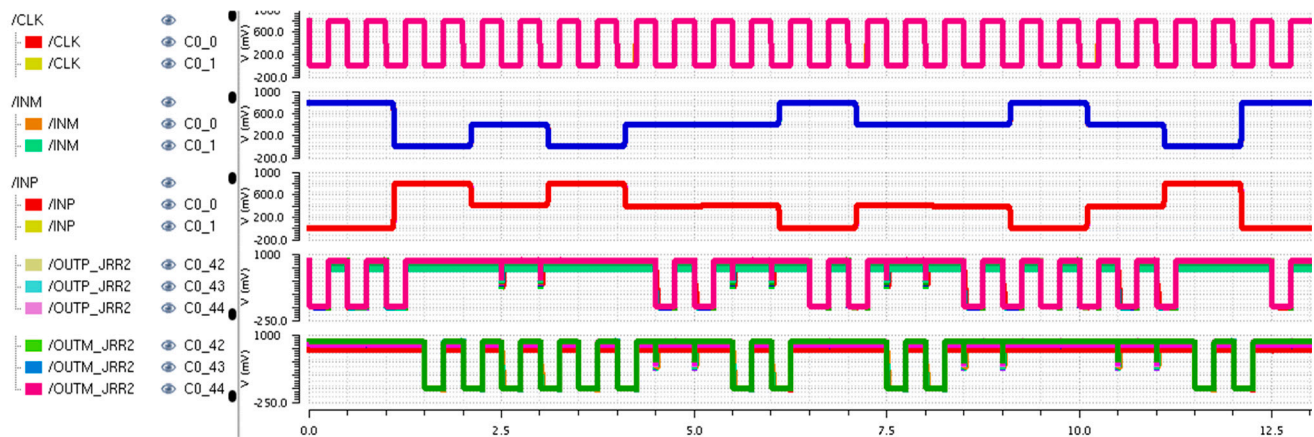


Figure 9. Schematic PVT Simulation of the proposed JRR2 Comparator Across 45 PVT Corners.

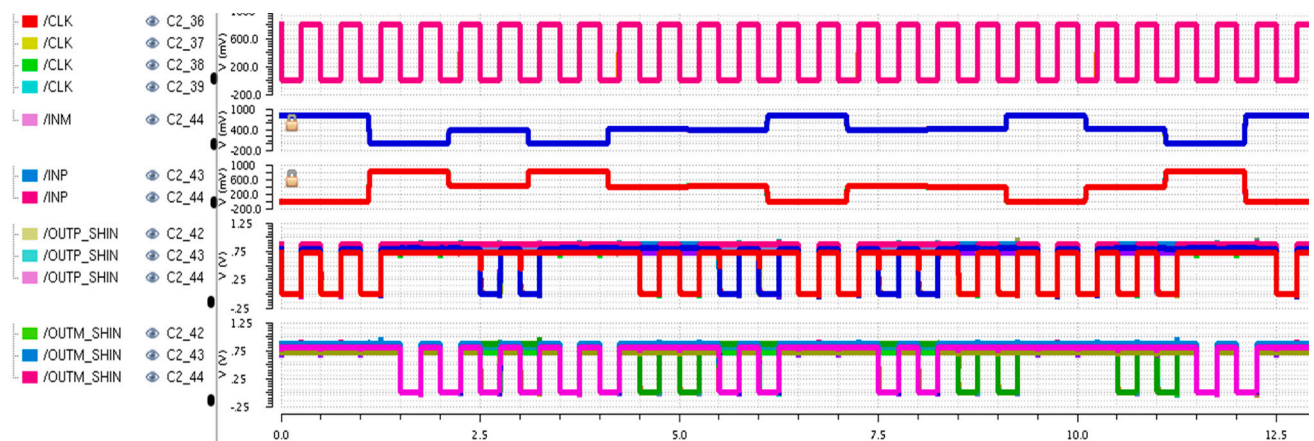


Figure 10. Schematic PVT Simulation of the Shin Comparator Across 45 PVT Corners.

Figure 11 presents the failed PVT corner simulation results identified by the proposed validation methodology for the Shin comparator, highlighting failures observed at the OUTM output node. The proposed test pattern successfully detected failures in 9 out of 45 PVT corner test configurations, particularly during test sequences 3, 5, 6, 8, 9, and 11. The failures occurred when the differential input voltage (ΔV_{in}) transitioned from Big Positive (BP, +800 mV) to Small Positive (SP, +0.8 mV) and Small Negative (SN, −0.8 mV) in test sequences 3 and 5, from Big Negative (BN, −800 mV) to SP and SN in test sequences 8 and 11, and between SN and SP in test sequences 6 and 9. These transitions involve near-zero differential input voltages and represent critical operating conditions for comparator decision-making.

Most failures were observed at the FS process corner, where the NMOS transistor operates with high mobility while the PMOS transistor operates with low mobility. Under this condition, the weakened PMOS transistor requires a longer regeneration time, leading to failures during the rapid ΔV_{in} transitions occurring within a 0.5 μ s interval. Consequently, the comparator output is unable to resolve correctly and exhibits metastable behavior.

Additional failures were observed under the SS process corner, where both NMOS and PMOS transistors operate with low mobility at a reduced supply voltage of 720 mV and a temperature of 0 °C. These conditions reduce the gain of the input latch and increase the comparator decision time. Furthermore, reduced decision robustness was observed in test sequences 3, 5, 6, 8, 9, and 11, particularly under the FS and SS process corners. Failures were also detected under the Typical process corner for test configuration 8 (VDD = 720 mV, 100 °C) and test configuration 9 (VDD = 800 mV, 0 °C). These results demonstrate that the proposed validation methodology is effective in identifying vulnerable PVT operating conditions and revealing comparator failures that occur during critical ΔV_{in} transitions.

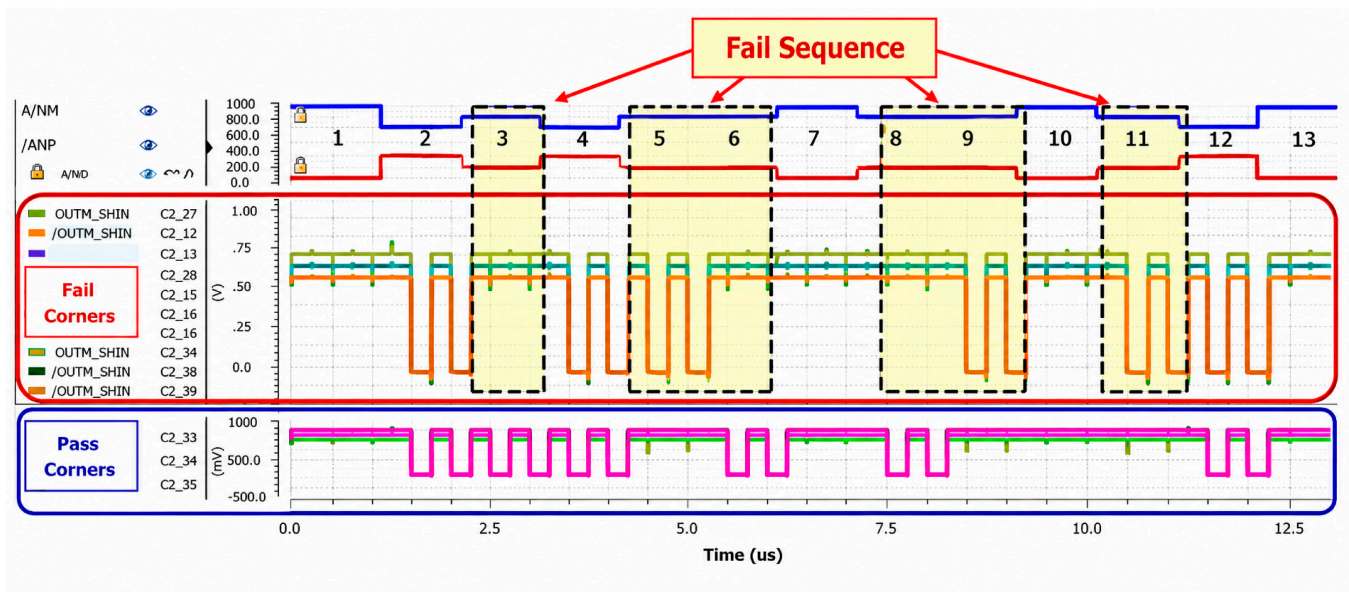


Figure 11. Failed Schematic PVT Simulation of the Shin Comparator Identified using the Proposed ITP Validation Methodology.

4.2. PVT Post-Layout Simulation

PVT analysis is more critical for post-layout designs due to the additional parasitic capacitances and resistances introduced during physical implementation. Figure 12 presents the post-layout PVT corner simulation results of the JRR2 comparator, which successfully passed all 45 PVT corner test configurations using the proposed ITP, demonstrating its robustness against PVT variations. In contrast, Figure 13 shows the post-layout simulation results of the Paik comparator, which failed in 8 out of 45 PVT corners, as summarized in Table 4 and highlighted in Figure 14.

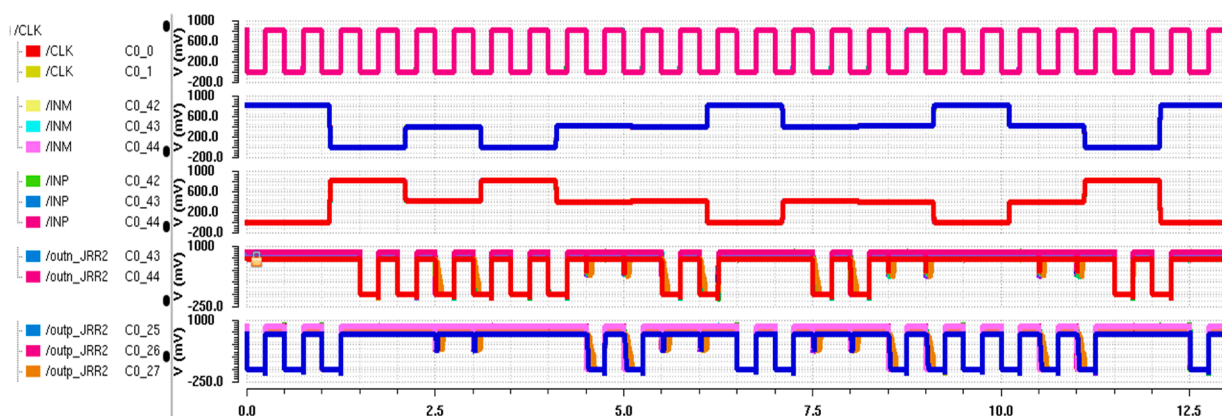


Figure 12. Post-layout PVT Simulation of the JRR2 Comparator Across 45 PVT Corners.

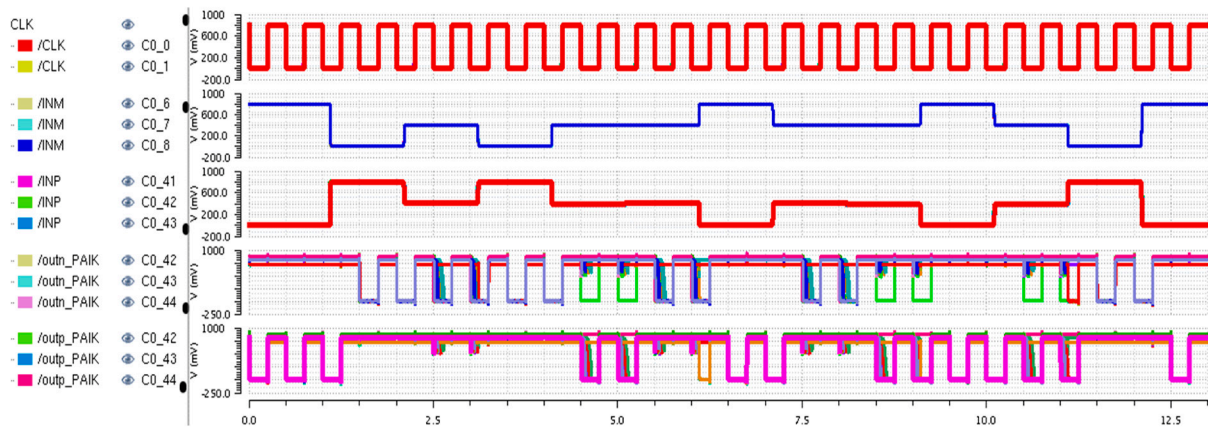


Figure 13. Post-layout PVT Simulation of the Paik Comparator Across 45 PVT Corners.

Table 4. List of Failed Process Corner in PVT Post-layout Simulation for the Paik Comparator.

No	Process Corner Test	NMOS	PMOS
1	C0_6_FF; 880 mV; 0 °C	High mobility	High mobility
2	C0_9_FS; 720 mV; 0 °C	High mobility	Low mobility
3	C0_10_FS; 720 mV; 30 °C	High mobility	Low mobility
4	C0_11_FS; 720 mV; 100 °C	High mobility	Low mobility
5	C0_12_FS; 800 mV; 0 °C	High mobility	Low mobility
6	C0_13_FS; 800 mV; 30 °C	High mobility	Low mobility
7	C0_14_FS; 800 mV; 100 °C	High mobility	Low mobility
8	C0_15_FS; 880 mV; 0 °C	High mobility	Low mobility
9	C0_16_FS; 880 mV; 30 °C	High mobility	Low mobility

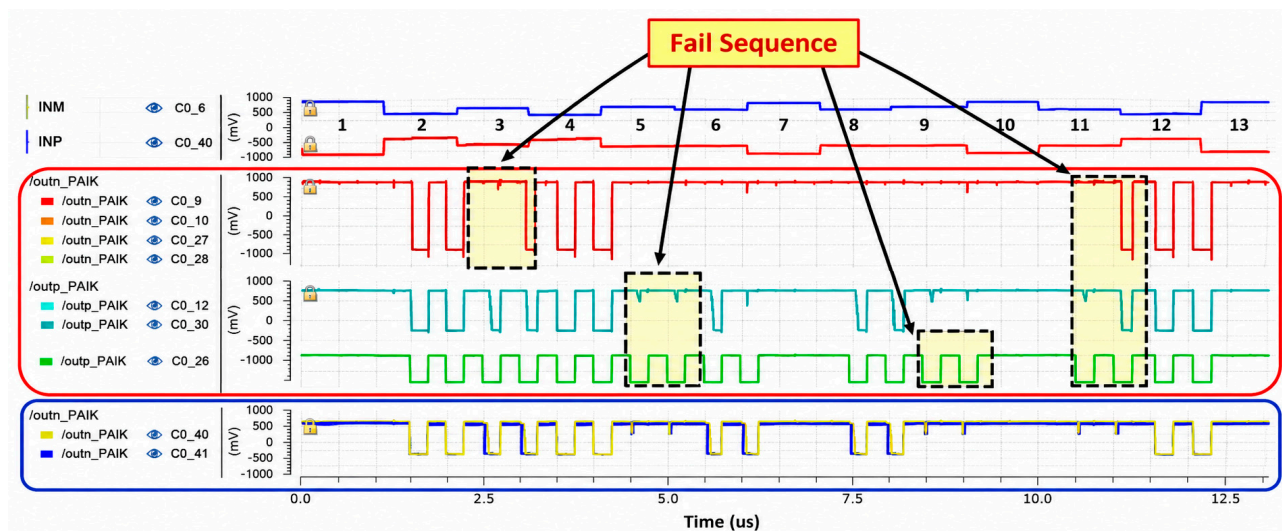


Figure 14. Failed Post-layout PVT Corner Simulation of the Paik Comparator.

The results indicate that configurations 1, 2, 5, and 6, corresponding to low-mobility PMOS conditions with $V_{DD} = 720$ mV, failed during test sequence 3 (transition from BP to SP) and test sequence 11 (transition from BN to SN). These failures suggest that the comparator exhibited difficulty in resolving transitions from large differential input voltages to near-zero differential input voltages under unfavourable operating conditions. Similarly, configurations 3 and 7, operating at $V_{DD} = 800$ mV with low-mobility PMOS transistors, failed during test sequences 5 and 11. Configuration 4, operating at $V_{DD} = 880$ mV with low-mobility NMOS transistors, failed during test sequences 5, 9, and 11, including the transition from

SP to SN. The failures observed in Figure 14 demonstrate that the proposed PVT validation methodology can identify vulnerable operating conditions that become more pronounced after layout extraction. The additional parasitic effects introduced during the layout stage increase the comparator decision time and reduce the regeneration margin, making the circuit more susceptible to failure during critical input transitions involving small differential voltages.

Overall, the results indicate that the Paik comparator is particularly vulnerable under FS process corner conditions, where the NMOS transistors operate with high mobility while the PMOS transistors operate with low mobility. As shown in Table 4, eight out of the nine failed PVT corners occurred under FS conditions across different supply voltages and temperatures. The failures were mainly observed during transitions from large differential input voltages (BP or BN) to near-zero differential input voltages (SP or SN), as well as polarity reversals between SP and SN. These critical transitions reduce the available regeneration time and increase the likelihood of incorrect output decisions. The results demonstrate that the proposed PVT validation methodology is effective in identifying weak operating corners and revealing post-layout performance degradation caused by process variations, supply voltage fluctuations, temperature changes, and layout parasitics.

The post-layout PVT simulation results for the Shin comparator, shown in Figure 15 and detailed in Figure 16 and Table 5, reveal significant performance degradation under several PVT conditions. A total of seven failed process corners were identified, with most failures occurring under FS and SS process corners. The FS corner conditions, where the NMOS transistor operates at high mobility and the PMOS transistor operates at low mobility, introduce a significant imbalance in the regenerative latch, resulting in reduced regeneration margin and a higher susceptibility to metastability during critical input transitions. Similarly, failures were observed under SS conditions, where both NMOS and PMOS transistors operate with low mobility, leading to reduced gain and slower decision-making capability. In contrast, the proposed JRR2 comparator maintained correct functionality across all post-layout PVT corner simulations, demonstrating superior robustness against PVT variations. The results confirm that the proposed PVT validation methodology is capable of identifying vulnerable operating conditions and exposing post-layout weaknesses that may compromise comparator reliability. Overall, the JRR2 comparator exhibits significantly improved tolerance to PVT variations compared to the Shin comparator, making it a more reliable solution for low-voltage and variation-aware applications.

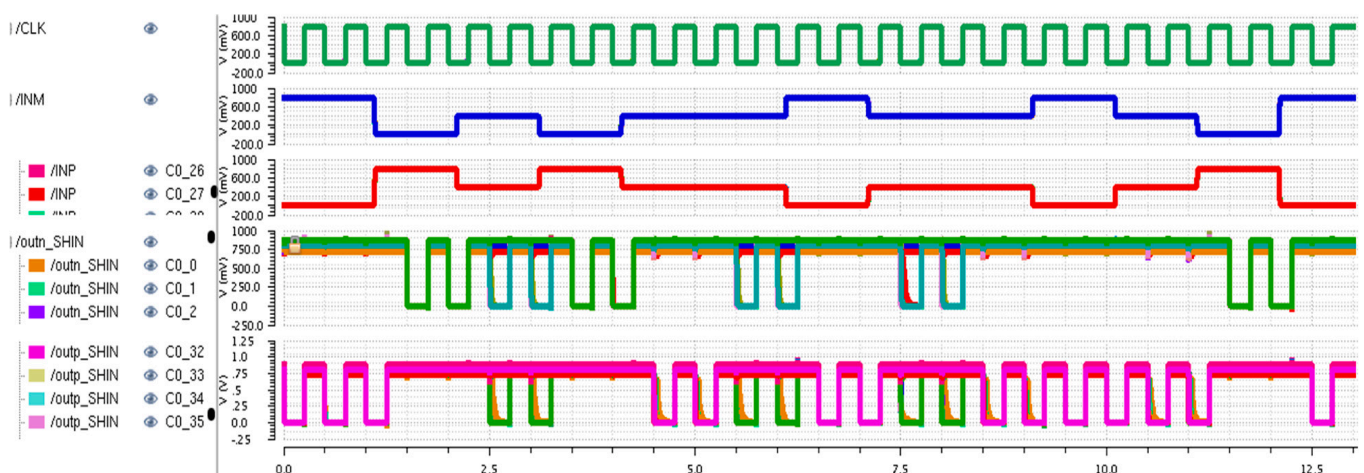


Figure 15. Post-layout PVT Simulation of the Shin Comparator Across 45 PVT Corners.

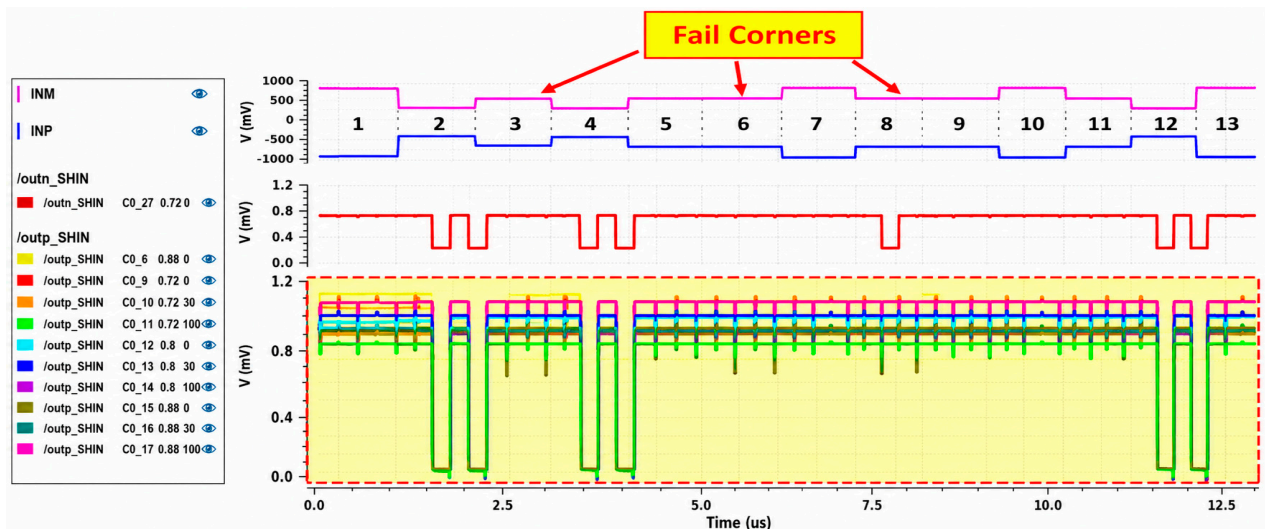


Figure 16. Failed Post-layout PVT Corner Simulation of the Shin Comparator.

Table 5. List of Failed Process Corner in PVT Post-Layout Simulation for Shin Comparator.

No	Process Corner Test	NMOS	PMOS
1	C0_9_FS; 720 mV; 0 °C	High mobility	Low mobility
2	C0_10_FS; 720 mV; 30 °C	High mobility	Low mobility
3	C0_12_FS; 800 mV; 0 °C	High mobility	Low mobility
4	C0_26_SF; 880 mV; 100 °C	Low mobility	High mobility
5	C0_27_SS; 720 mV; 0 °C	Low mobility	Low mobility
6	C0_28_SS; 720 mV; 30 °C	Low mobility	Low mobility
7	C0_30_SS; 800 mV; 0 °C	Low mobility	Low mobility

4.3. Failure Mechanisms of Existing Architectures

The post-layout PVT simulation results reveal significant differences in robustness among the evaluated comparator architectures. The failures observed in the Shin comparator are primarily attributed to mobility imbalance under FS and SS process corners, where the mismatch between NMOS and PMOS switching characteristics reduces the differential gain available for latch regeneration. Under these conditions, the comparator becomes more susceptible to metastability, particularly during transitions involving small differential input voltages. Similarly, the Paik comparator exhibits failures under several PVT conditions due to premature latch regeneration before sufficient differential voltage gain is established by the dynamic amplifier stage. This behavior increases sensitivity to kickback-induced disturbances and limits reliable operation under low-voltage conditions. In contrast, the proposed JRR2 comparator successfully satisfies the design specifications across all evaluated PVT corners. The threshold-controlled latch activation mechanism delays regeneration until sufficient differential voltage gain is developed, thereby reducing metastability probability and improving robustness against PVT variations. This behavior contributes significantly to the superior reliability observed during both schematic and post-layout PVT validation.

4.4. Delay Analysis

Regeneration delay is one of the most critical performance metrics in dynamic comparators because it directly determines the maximum operating speed and conversion rate of SAR ADCs. Under low-voltage operation, small differential input signals may cause prolonged regeneration times and increase the likelihood of metastability, particularly under unfavorable PVT conditions. Therefore, minimizing regeneration delay while maintaining

robust operation is essential for achieving reliable high-speed comparator performance. This section first presents the delay analysis methodology used to evaluate the comparator architectures. Subsequently, the regeneration and reset delay performances of the proposed JRR2 comparator are compared with the Shin, Paik, and JRR1 comparators under nominal operating conditions. Finally, the delay performance of the proposed design is investigated under 45 PVT corner simulations at both schematic and post-layout levels to assess its robustness against manufacturing and environmental variations.

4.4.1. Delay Analysis Methodology

Delay performance is a critical parameter in dynamic comparators because excessive regeneration delay may lead to metastability and incorrect SAR conversion decisions. In low-voltage dynamic comparators, small differential input voltages may lead to metastable conditions where the output nodes require a longer time to resolve to valid logic levels. Excessive delay can degrade the conversion speed of SAR ADCs and increase the probability of decision errors. Therefore, regeneration delay is a critical performance parameter for evaluating comparator robustness and operating speed under PVT variations [26–28]. To analyze the delay performance across PVT variations, detailed simulations were conducted in both schematic and post-layout designs. To evaluate the performance of the proposed comparators, simulations were conducted with same simulation setup and the transistor sizes were uniformly scaled to ensure equal parasitic capacitance and resistance. The input setup used during the simulations are 800 mV to 0.8 mV to assess critical delay metrics. In dynamic comparators, propagation delay arises during the regeneration and reset phases.

In dynamic comparators, the total regeneration delay consists of two components: the pre-amplifier delay (t_{amp}) and the latch delay (t_{latch}), as indicated in Equation (2). The pre-amplifier delay is the time needed for the load capacitance (C_L) at the latch stage output to reach the threshold that activates the first NMOS transistor, initiating latch regeneration. The latch delay corresponds to the time for cross-coupled inverters to achieve a voltage swing of $\Delta V_{out} = V_{DD}/2$ from an initial voltage difference (ΔV_0). The total dynamic comparator delay is described by Equation (2).

$$t_{delay} = t_{amp} + t_{latch} \quad (2)$$

t_{amp} represents the capacitive charging of the load capacitance (C_L) at the latch stage output nodes Outn and Outp until the first NMOS transistor inverter turns ON and the latch regeneration starts. The charging delay (t_{amp}) given by Equation (3) below.

$$t_{amp} = 2 \frac{V_{Thn} C_{Lout}}{I_{tail}} \quad (3)$$

$$t_{latch} = \frac{C_L}{g_{m, eff}} \cdot \ln \left(\frac{\Delta V_{out}}{\Delta V_0} \right) \quad (4)$$

$$t_{latch} = \frac{C_L}{g_{m, eff}} \cdot \ln \left(\frac{V_{DD}/2}{\Delta V_0} \right) \quad (5)$$

The second term, (t_{latch}) as in Equation (4) is the latching delay of two cross-coupled inverters. The voltage swing of $\Delta V_{out} = V_{DD}/2$ has to be obtained from an initial output voltage difference ΔV_0 at the falling Outp/Outn. Half of the supply voltage is considered to be the threshold voltage of the comparator following the inverter [24]. Hence the final equation for t_{latch} is expressed in Equation (5). The ΔV_0 depends strongly on the transconductance of the input transistor and the pre-amplifier stage, ΔV_{in} , latch tail current, and the capacitive ratio of capacitive load at output latch (C_{Llatch}) to capacitive load to

output pre-amplifier stage (C_{Lamp}). The total delay of the dynamic comparator is denoted as in Equation (6) below.

$$t_{delay} = 2 \frac{V_{Thn} C_{Lout}}{I_{tail}^2} + \frac{C_L}{g_{m, eff}} \cdot \ln \left(\frac{V_{DD}/2}{\Delta V_0} \right) \quad (6)$$

4.4.2. Delay Analysis for JRR2 Comparator

Figure 17 presents the nominal simulation results for the regeneration delay of several comparators with a differential input of $\Delta V_{in} = 800$ mV. The JRR2 comparator achieves the shortest regeneration delay at 327 ps, significantly outperforming the other comparators: JRR1 with 411 ps, Shin with 463 ps, and Paik with 494 ps. This represents a performance improvement of approximately 20% over JRR1, 30% over Shin, and 33% over Paik, clearly establishing JRR2 as the most efficient design in terms of speed. The larger improvement over the Shin and Paik comparators indicates that the proposed architecture establishes a higher initial differential voltage before latch regeneration begins. Consequently, the regenerative latch enters positive feedback more rapidly, thereby shortening the overall regeneration time. The reduced regeneration delay is attributed to the proposed threshold-controlled latch activation mechanism, which postpones latch regeneration until sufficient differential voltage amplification is established. Consequently, the comparator accelerates positive feedback during regeneration while reducing the probability of metastability under low-voltage operation. Additionally, while the JRR1 and Shin comparators offer reasonable performance improvements over the Paik comparator, they are clearly outperformed by JRR2 in terms of regeneration speed.

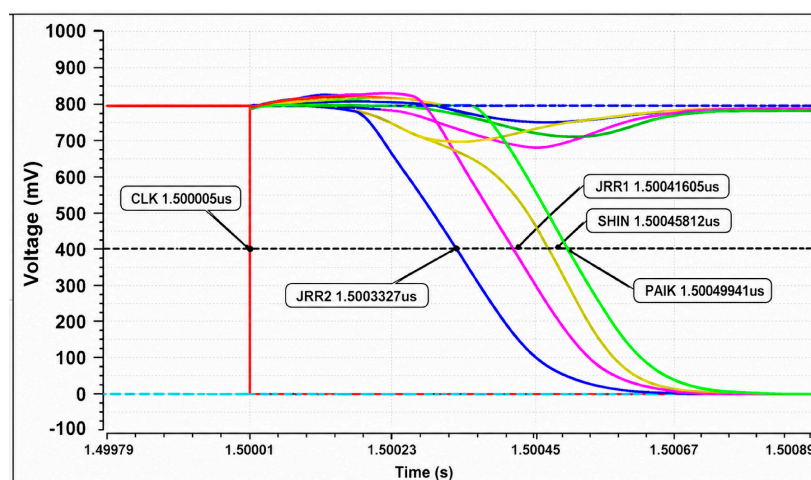


Figure 17. Comparison of Regeneration Delay at Nominal Condition with $\Delta V_{in} = 800$ mV.

In Figure 18, JRR2 consistently delivers the best regeneration performance, particularly at higher voltage differences, where it stabilizes at 0.4 ns from 500 mV to 1800 mV. While Shin and JRR1 perform similarly, especially at higher voltages, Shin has a slight advantage at lower voltages. Paik, on the other hand, exhibits the highest delays across all voltage levels, making it the slowest comparator. The performance gap between JRR2 and Paik is especially pronounced at higher voltages, solidifying JRR2 as the most efficient option. The proposed JRR2 comparator consistently outperforms the Paik comparator, achieving regeneration delay improvements ranging from 10% at $\Delta V_{in} = 0.4$ mV to over 32% at $\Delta V_{in} = 50$ mV and 100 mV. For differential input voltages above 300 mV, the proposed comparator maintains a consistent improvement of approximately 25–32%, demonstrating stable regeneration performance over a wide input-voltage range.

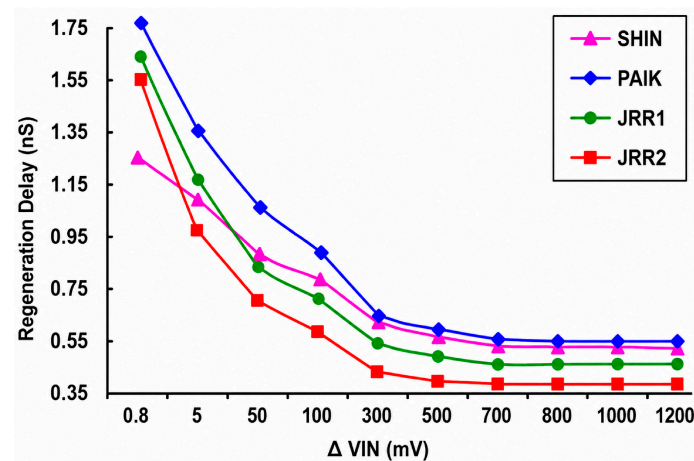


Figure 18. The regeneration delay at nominal condition.

The relatively constant improvement observed at higher differential input voltages suggests that the regeneration process becomes less dependent on the input amplitude once sufficient differential gain has been established. This behaviour is desirable for SAR ADC operation because it provides more predictable comparator timing throughout the successive approximation process. This improvement is achieved because the dynamic amplifier stage establishes a larger differential voltage before latch regeneration begins, allowing the regenerative latch to enter positive feedback with a stronger initial voltage difference. Consequently, the latch reaches the final logic state more rapidly while reducing the sensitivity of regeneration delay to variations in the input differential voltage. This behaviour is particularly beneficial for SAR ADC operation because it provides more predictable comparator timing throughout the successive approximation process.

Figure 19 illustrates the reset delays for the same configurations. JRR2 once again delivers the best performance, maintaining the lowest reset delay values across all voltage differences. Schinkel shows the highest reset delays, followed by Paik and JRR1, while JRR2 remains stable with delays ranging from 154–157 ps across all voltage levels. Shinkel's reset delays increase significantly as the input voltage difference rises, reaching 430 ps. In terms of percentage improvement, JRR2 outperforms Schinkel by 45–64%, with the largest improvements observed at higher voltage differences (500 mV and above). Similarly, JRR2 consistently outperforms Paik with a 20–23% improvement. This steady performance of JRR2 across various input voltages further reinforces its position as the most efficient comparator configuration, excelling in both regeneration and reset delay characteristics. The nearly constant reset delay observed across the evaluated differential input voltage range indicates that the reset operation is less sensitive to input signal amplitude. Such behaviour enables the comparator to recover rapidly before the next comparison cycle, thereby supporting high-speed SAR ADC operation.

4.4.3. Delay Performance of Schematic Designs in 45 PVT Corner Simulation

Figure 20 illustrates the output of the dynamic amplifier, showing that each time the input signals (INP and INM) toggle, the output signals (OUTP_JRR2 and OUTM_JRR2) stabilize before the clock (CLK) signal transitions to HIGH. The simulation results demonstrate a longer regeneration delay of 927 ps under the conditions of $V_{DD} = 720$ mV, temperature = 0 °C, and the SS process corner. This delay is attributed to limited voltage headroom, a 10% reduction in V_{DD} , and the slower mobility of electrons at 0 °C. Conversely, the regeneration delay decreases to 189 ps under conditions of $V_{DD} = 880$ mV, temperature = 100 °C, and the FF process corner. The higher supply voltage and increased carrier mobility under the FF process corner accelerate

the regeneration process by increasing the transconductance of the regenerative latch, thereby reducing the overall decision time.

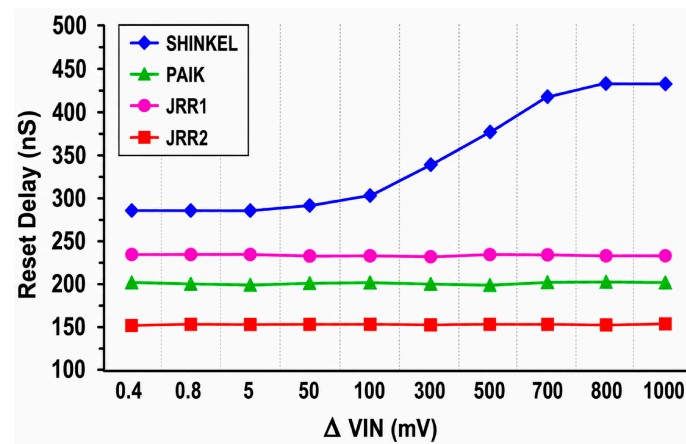


Figure 19. The Reset delay at nominal condition.

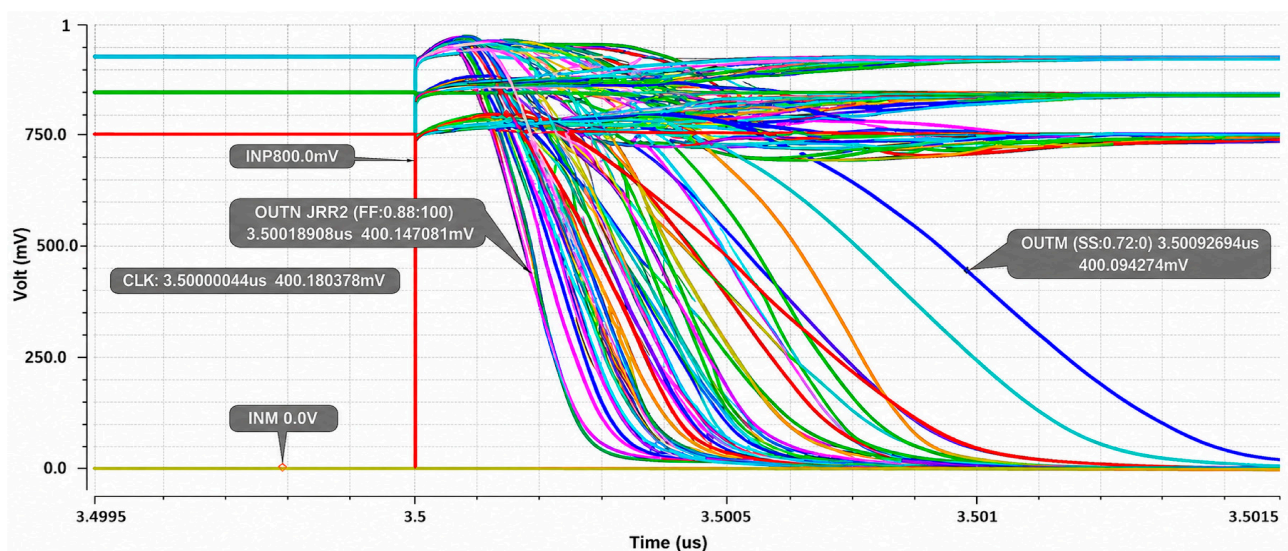


Figure 20. Regeneration Delay of Schematic JRR2 Comparator with $\Delta V_{in} = 800$ mV Across 45 PVT Corner Simulation.

Table 6 presents a comparative analysis of the regeneration delay performance for four different comparator configurations: Shin, Paik, JRR1, and JRR2. The analysis focuses on both maximum and minimum regeneration delays under varying conditions of input ΔV_{in} , V_{DD} , temperature, and process corners. This comparative evaluation aims to identify the most suitable comparator design for high-precision, low-voltage applications. At a high input voltage difference of 800 mV, the JRR2 comparator consistently demonstrates the shortest delays, indicating superior efficiency in resolving the input voltage difference compared to the other designs. The improvement becomes more evident under the SS process corner and reduced supply voltage because latch regeneration is more susceptible to limited transistor drive capability under subthreshold operation. By allowing greater differential voltage amplification before regeneration, the proposed architecture alleviates this limitation and maintains faster decision making. For instance, under the worst-case scenario of $V_{DD} = 720$ mV, temperature = 0°C , and SS process corner, the JRR2 exhibits a maximum delay of 0.93 ns, outperforming the Shin, Paik, and JRR1 comparators by 33%, 39%, and 24%, respectively.

Table 6. Performance Comparison of Delay in PVT Schematic Simulation.

Comparator Configuration	Shin	Paik	JRR1	JRR2
Max Regeneration Delay $\Delta V_{in} = 800 \text{ mV}$ $V_{DD} = 720 \text{ mV}$; Temp. = 0°C ; Process = SS;	1.39 ns	1.52 ns	1.22 ns	0.93 ns
Min Regeneration Delay $\Delta V_{in} = 800 \text{ mV}$; $V_{DD} = 880 \text{ mV}$; Temp. = 100°C ; Process = FF;	296 ps	267 ps	220 ps	189 ps
Max Regeneration Delay $\Delta V_{in} = 0.8 \text{ mV}$ $V_{DD} = 720 \text{ mV}$; Temp. = 0°C ; Process = SS;	Fail 9 corners	31 ns	27 ns	29 ns
Min Regeneration Delay $\Delta V_{in} = 0.8 \text{ mV}$; $V_{DD} = 880 \text{ mV}$; Temp. = 100°C ; Process = FF;	Fail 9 corners	511 ps	472 ps	582 ps

Similarly, at the minimum delay condition of $V_{DD} = 880 \text{ mV}$, temperature = 100°C , and FF process corner, the JRR2 achieves the lowest delay of 189 ps, a 36% improvement over Shin, 29% over Paik, and 14% over JRR1. However, when dealing with a small input voltage difference of 0.8 mV, the performance of all comparators is compromised, with the Shin comparator failing to operate effectively under these conditions. The JRR1 comparator shows promising results in low input voltage scenarios, surpassing the JRR2 in terms of minimum delay for $\Delta V_{in} = 0.8 \text{ mV}$ conditions. Specifically, JRR1 exhibits a minimum delay of 472 ps, outperforming JRR2 by 19% under the same conditions of $V_{DD} = 880 \text{ mV}$, temperature = 100°C , and FF process corner. Although the JRR1 comparator achieves a shorter regeneration delay under this specific nominal operating condition, delay alone is insufficient for evaluating comparator performance. Practical SAR ADC operation also requires robust functionality over wide process, voltage, and temperature variations, where the proposed JRR2 comparator consistently maintains successful operation across all evaluated PVT conditions.

Overall, the proposed JRR2 comparator achieves the best compromise between regeneration speed and PVT robustness. This result demonstrates that evaluating comparator performance solely under nominal conditions may lead to misleading conclusions, whereas comprehensive PVT verification provides a more realistic assessment of practical circuit robustness. Although the JRR1 comparator exhibits a slightly shorter delay under one nominal low-input condition, it does not maintain the same level of robustness across the evaluated PVT corners. In contrast, the proposed JRR2 comparator successfully maintains reliable operation across all 45 PVT-corner simulations, demonstrating superior suitability for low-voltage SAR ADC applications.

4.4.4. Delay Performance of Post-Layout Designs in 45 PVT Corner Simulation

The regeneration delay in post-layout designs is generally longer compared to schematic designs due to the impact of parasitic capacitors and resistors, emphasizing the need for careful layout optimization. Figure 21 illustrates the regeneration time of the JRR2

comparator under post-layout conditions, with input differences of $\Delta V_{in} = 800$ mV and $\Delta V_{in} = 0.8$ mV. The simulation results indicate an increase in delay as the input difference decreases. For a large input difference ($\Delta V_{in} = 800$ mV), the optimized regeneration delay of 1.6 ns was achieved at $V_{DD} = 0.72$ V, Temperature = 0 °C, and SS process corner. The analysis of the delay performance of the comparators in post-layout PVT simulations listed in Table 7 reveals that the JRR2 comparator consistently exhibits optimal performance across all configurations during the regeneration delay.

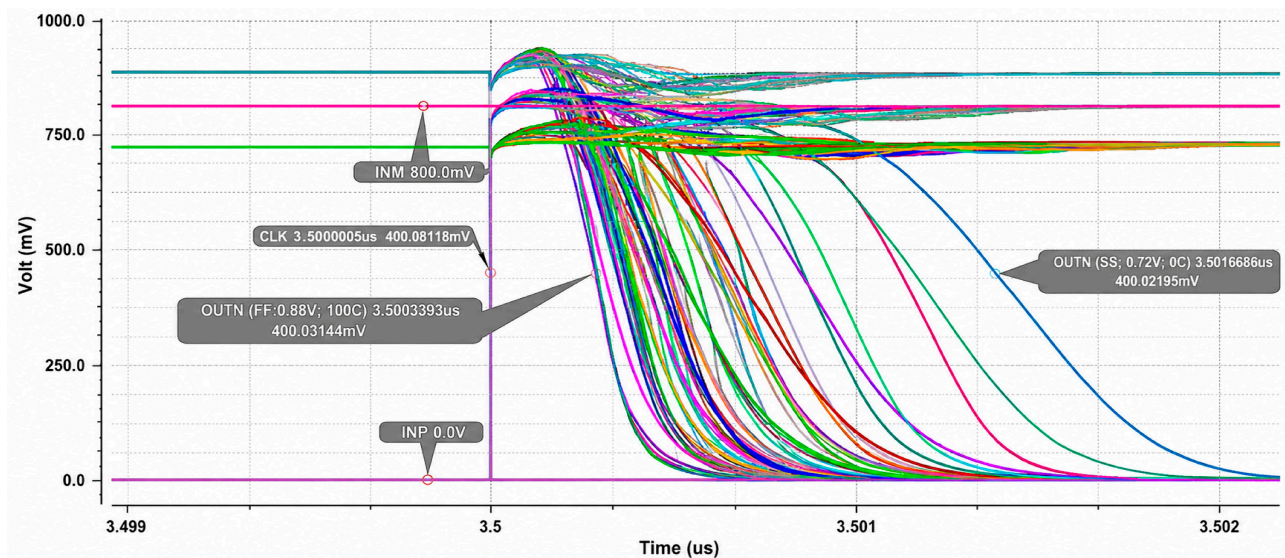


Figure 21. Regeneration Delay of Post-layout JRR2 Comparator with $\Delta V_{in} = 800$ mV Across 45 PVT Corner Simulation.

Table 7. Performance Comparison of Regeneration Delays in PVT Post-Layout Simulation.

Comparator Configuration	Shin	Paik	JRR1	JRR2
Max regeneration delay $\Delta V_{in} = 800$ mV $V_{DD} = 720$ mV; Temp. = 0 °C; Process = SS;	1.7 ns	2.8 ns	1.9 ns	1.6 ns
Min regeneration delay $\Delta V_{in} = 800$ mV; $V_{DD} = 880$ mV; Temp. = 100 °C; Process = FF;	378 ps	418 ps	321 ps	333 ps
Max regeneration delay $\Delta V_{in} = 0.8$ mV $V_{DD} = 720$ mV; Temp. = 0 °C; Process = SS;	Fail 9 corners	Fail 7 corners	113 ns	105 ns
Min regeneration delay $\Delta V_{in} = 0.8$ mV; $V_{DD} = 880$ mV; Temp. = 100 °C; Process = FF;	Fail 9 corners	Fail 7 corners	1 ns	1 ns

Specifically, the JRR2 demonstrates the shortest maximum regeneration delay of 1.6 ns and an impressive minimum delay of 333 ps under high input voltage conditions, significantly outperforming the Shin and Paik comparators, which experience considerable delays of 1.7 ns and 2.8 ns for maximum delays and 378 ps and 418 ps for minimum delays, respectively. This corresponds to regeneration-delay reductions of approximately 6%, 43%, and 20% compared with the JRR1, Paik, and Shin comparators, respectively, under the worst-case post-layout operating condition. In scenarios involving a low input voltage difference of 0.8 mV, both the Shin and Paik comparators fail to operate effectively under critical PVT conditions, while JRR1 and JRR2 show delays of 113 ns and 105 ns, respectively. The 7.1% reduction in regeneration delay achieved by the proposed JRR2 comparator after layout extraction indicates that the performance advantage is preserved despite the additional parasitic capacitances and resistances introduced during physical implementation. This demonstrates that the proposed architecture maintains its effectiveness under practical implementation conditions. The limited increase in regeneration delay after layout extraction further indicates that the proposed architecture is relatively insensitive to layout parasitics, which is advantageous for practical integrated circuit implementation.

These results demonstrate that the proposed comparator preserves both fast regeneration and robust functionality after layout extraction, confirming that the threshold-controlled latch activation mechanism remains effective despite the presence of layout parasitics. Overall, the findings indicate that the JRR2 comparator is well-suited for high-precision, low-voltage applications, highlighting its advantages. The post-layout results further confirm that the proposed threshold-controlled latch activation mechanism remains effective after layout extraction, despite the additional parasitic capacitances and resistances introduced during physical implementation.

4.5. Power Analysis

Power consumption is a key performance metric in dynamic comparators, particularly for low-power SAR ADC applications where energy efficiency directly affects battery life and overall system performance. Since the comparator is the primary analog decision-making block in a SAR ADC, minimizing its power consumption is essential for extending battery lifetime and improving overall converter energy efficiency. Since dynamic comparators operate without static bias currents, their power consumption is primarily determined by the charging and discharging of internal and parasitic capacitances during clock transitions. Consequently, power consumption is strongly influenced by operating conditions such as supply voltage, differential input voltage, and PVT variations. Therefore, a comprehensive power analysis is required to evaluate both the energy efficiency and robustness of the proposed comparator architecture. This section first presents the power analysis methodology, followed by an investigation of the effects of V_{DD} and differential input voltage (ΔV_{in}) on power consumption under nominal operating conditions. Subsequently, the average power consumption of the proposed JRR2 comparator is evaluated under 45 PVT corner simulations at both schematic and post-layout levels and compared with the Shin, Paik, and JRR1 comparator architectures.

4.5.1. Power Analysis Methodology

Power consumption is a critical performance metric in dynamic comparators, particularly for low-power SAR ADC applications operating under stringent energy constraints. Since the proposed comparator is implemented using a fully dynamic architecture without static bias currents, its power consumption is primarily associated with the charging and discharging of internal and parasitic capacitances during clock transitions [29,30]. Consequently, power consumption is strongly influenced by supply voltage, switching activity,

and PVT variations. Evaluating power consumption under different operating conditions is therefore essential for assessing both the energy efficiency and robustness of the proposed comparator architecture.

The following analysis investigates the influence of supply voltage, differential input voltage (ΔV_{in}), and PVT variations on the average power consumption of the proposed comparator. In this work, the transistors were optimized to operate at a supply voltage of 0.8 V with a target SAR ADC clock frequency of 2 MHz. The results indicate that supply voltage, differential input voltage (ΔV_{in}), and temperature variations significantly influence the overall power consumption. Since dynamic comparators operate under periodic switching conditions, average power consumption (APC) is widely adopted as the primary performance metric because it inherently includes both dynamic charging/discharging current and short-circuit current components measured from the supply source during transient operation.

The average power consumption was calculated using the transient supply current obtained from Cadence Virtuoso Visualization Analysis XL according to:

$$APC = (\text{average}(I_T(V_{DD})) \times 0.8) \quad (7)$$

where $I_T(V_{DD})$ represents the transient current drawn from the supply source and V_{DD} is the supply voltage.

To evaluate the energy efficiency of the comparator, the figure-of-merit (FoM) was calculated using Equation (8). The FoM is calculated based on the comparator evaluation frequency, following the convention adopted in comparator literature such as Refs. [17,24,30].

$$FoM = \frac{P_{avg}}{f_{clk}} \quad (8)$$

where P_{avg} is the average power consumption and f_{clk} is the clock frequency. A lower FoM indicates better energy efficiency because less energy is consumed during each comparison step.

4.5.2. Nominal Power Analysis of the Proposed JRR2 Comparator

Figure 22 illustrates the variation in average power consumption with respect to the V_{DD} for the proposed JRR2, JRR1, Shin, and Paik comparators under nominal simulation conditions. The average power consumption was calculated using the transient supply current according to (7). As expected, the average power consumption decreases as the supply voltage is reduced because the dynamic switching energy is proportional to the charging and discharging of the internal capacitances. Although reducing V_{DD} effectively lowers power consumption, excessive supply voltage reduction decreases the available voltage headroom for the dynamic comparator, thereby degrading regeneration capability and potentially limiting the minimum resolvable differential input voltage. Based on the nominal simulation results, a supply voltage of 0.8 V was selected because it provides an effective balance between ultra-low-power operation and sufficient voltage headroom for reliable comparator operation. At this operating point, the proposed JRR2 comparator achieves an average power consumption of 41.4 nW while maintaining sufficient voltage headroom to reliably resolve a minimum differential input voltage of 0.8 mV, corresponding to $\frac{1}{2}$ LSB of the target 10-bit SAR ADC. The robustness of this operating point under manufacturing and environmental variations is further evaluated through the comprehensive 45 PVT corner simulations presented in the following sections.

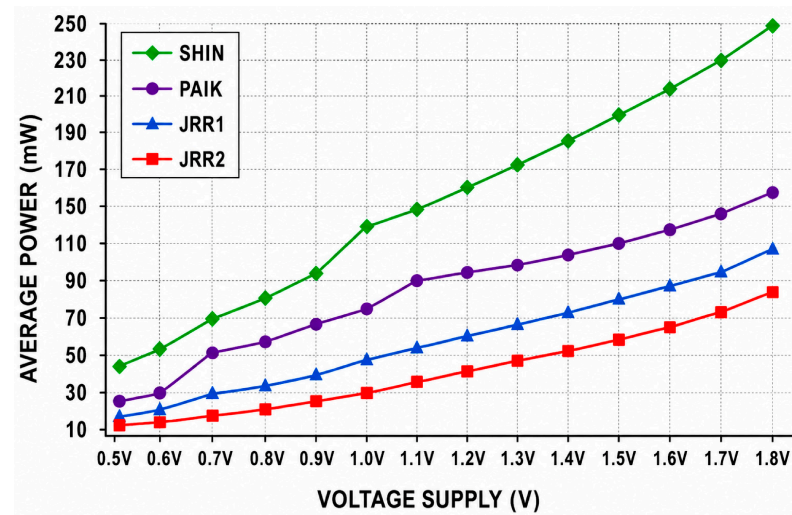


Figure 22. Average Power Consumption Across V_{DD} Variation.

Figure 23 presents the variation in average power consumption with respect to the differential input voltage (ΔV_{in}) under nominal operating conditions. During SAR conversion, the comparator must reliably resolve differential input voltages ranging from $\frac{1}{2}$ LSB (0.8 mV) to $\frac{1}{2}$ MSB (800 mV). Therefore, maintaining nearly constant average power consumption throughout this input range is desirable to ensure consistent energy efficiency during every comparison cycle. Among the evaluated architectures, the proposed JRR2 comparator exhibits the lowest and most stable average power consumption across the entire ΔV_{in} range. Even at the minimum differential input voltage of 0.8 mV, where regeneration is most susceptible to metastability and prolonged decision time, the proposed JRR2 comparator exhibits only minimal variation in average power consumption while maintaining reliable decision operation. This behaviour is attributed to the proposed threshold-controlled latch activation mechanism, which delays latch regeneration until sufficient differential voltage amplification is established by the dynamic amplifier stage. Consequently, unnecessary regenerative switching activity is minimized, enabling nearly constant energy consumption throughout the SAR conversion process despite large variations in differential input voltage.

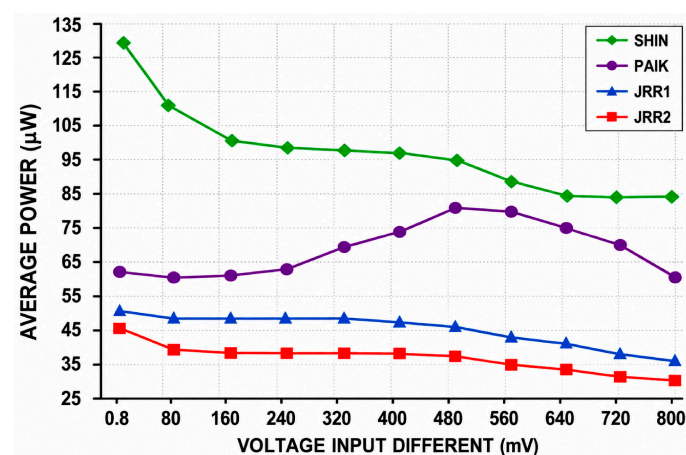


Figure 23. Average Power Consumption Across ΔV_{in} Variation.

The nominal average power consumption obtained from the proposed JRR2 comparator was used to calculate the energy-per-comparison figure-of-merit (FoM), which is widely

adopted for evaluating the energy efficiency of dynamic comparators. Using a sampling frequency of 2 MHz, the corresponding FoM is calculated as:

$$\text{FoM} = 41.4 \text{ nW} / 2 \text{ MHz} = 20.7 \text{ fJ/comparison-step}$$

Among the evaluated architectures, the proposed JRR2 comparator achieves the lowest average power consumption and the best energy efficiency under nominal operating conditions. The low FoM is attributed to the proposed threshold-controlled latch activation mechanism, which suppresses premature regeneration by delaying latch activation until sufficient differential voltage amplification is established. Consequently, unnecessary regenerative switching activity is minimized while reliable comparator operation is maintained. The robustness of this nominal operating point is further verified through the comprehensive 45 PVT corner simulations presented in the following sections.

4.5.3. Power Performance of Schematic Designs in 45 PVT Corner Simulation

Figure 24 illustrates the average power consumption of the proposed JRR2 comparator under all 45 schematic PVT corner simulations. As expected, the average power consumption increases with both supply voltage and temperature because higher transistor conduction and leakage currents increase the transient switching current drawn from the supply. Nevertheless, the proposed comparator consistently maintains nanowatt-level power consumption across all evaluated PVT conditions, ranging from 33 nW at the SS corner ($V_{DD} = 0.72 \text{ V}$, 0°C) to 68 nW at the FF corner ($V_{DD} = 0.88 \text{ V}$, 100°C). The relatively small variation in average power consumption across the evaluated PVT corners indicates that the proposed comparator maintains stable energy behaviour despite simultaneous process, supply-voltage, and temperature variations. These results indicate that the proposed comparator preserves stable energy characteristics despite simultaneous process, voltage, and temperature variations, confirming the effectiveness of the proposed threshold-controlled latch activation mechanism.

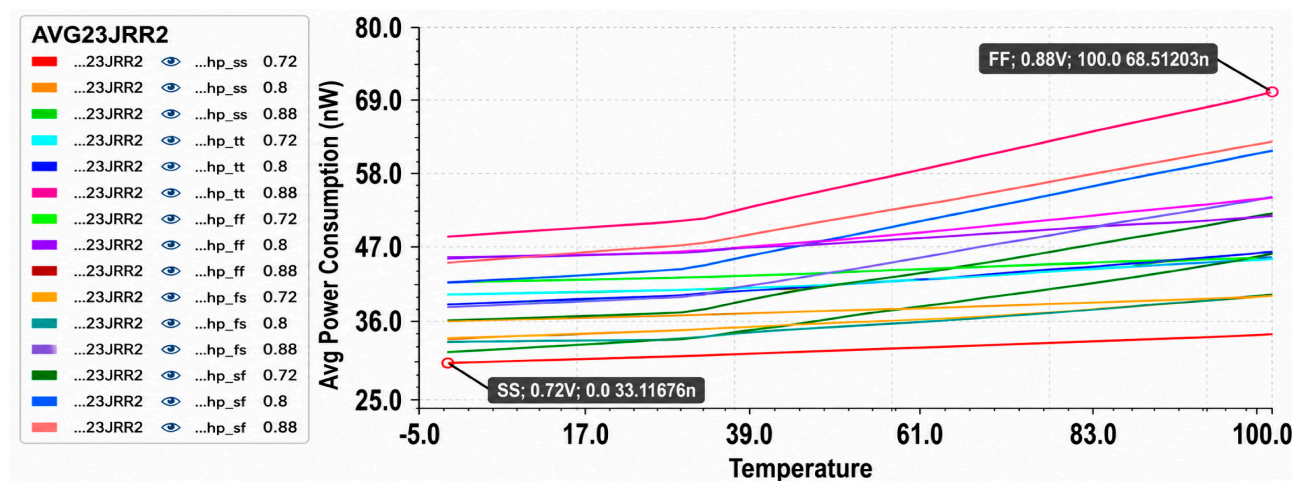


Figure 24. Average power consumption of the schematic JRR2 comparator under 45 PVT corner simulations.

Table 8 compares the schematic average power consumption of the Shin, Paik, JRR1, and proposed JRR2 comparators under identical PVT conditions. Among the evaluated architectures, the proposed JRR2 comparator achieves the lowest maximum and minimum average power consumption. At the worst-case operating condition (FF, $V_{DD} = 0.88 \text{ V}$, 100°C), the maximum average power consumption is limited to 68 nW, representing reductions of 72.7% and 77.3% compared with the Shin and Paik comparators, respec-

tively. Likewise, under the lowest-power operating condition (SS, $V_{DD} = 0.72$ V, 0 °C), the proposed comparator achieves a minimum average power consumption of 33 nW, corresponding to reductions of 61.6%, 25.0%, and 10.8% compared with the Shin, Paik, and JRR1 comparators, respectively. These results demonstrate that the proposed comparator maintains stable ultra-low-power operation across wide process, voltage, and temperature variations, confirming the effectiveness of the proposed threshold-controlled latch activation mechanism.

Table 8. Comparison of average power consumption under schematic PVT simulations.

Comparator Configuration	Shin	Paik	JRR1	JRR2
Max. Average Power $V_{DD} = 0.88$ V; Temp. = 100 °C; Process = FF	249 nW	300 nW	76 nW	68 nW
Min. Average Power $V_{DD} = 0.72$ V; Temp. = 0 °C; Process = SS	86 nW	44 nW	37 nW	33 nW

4.5.4. Power Performance of Post-Layout Designs in 45 PVT Corner Simulation

Figure 25 illustrates the average power consumption of the proposed JRR2 comparator under all 45 post-layout PVT corner simulations. Compared with the schematic implementation, the post-layout average power consumption increases because of the additional parasitic resistance and capacitance introduced during physical layout extraction. Nevertheless, the proposed comparator maintains ultra-low-power operation across all evaluated PVT corners, with the average power consumption ranging from 40.42 nW at the SS corner ($V_{DD} = 0.72$ V, 0 °C) to 108.38 nW at the FF corner ($V_{DD} = 0.88$ V, 100 °C). Although layout parasitic increases the overall power consumption compared with the schematic implementation, the relative variation across the evaluated PVT corners remains well controlled, indicating that the proposed architecture preserves its energy-efficient characteristics after physical implementation. These results confirm that the proposed comparator maintains reliable ultra-low-power operation across all evaluated post-layout PVT corners.

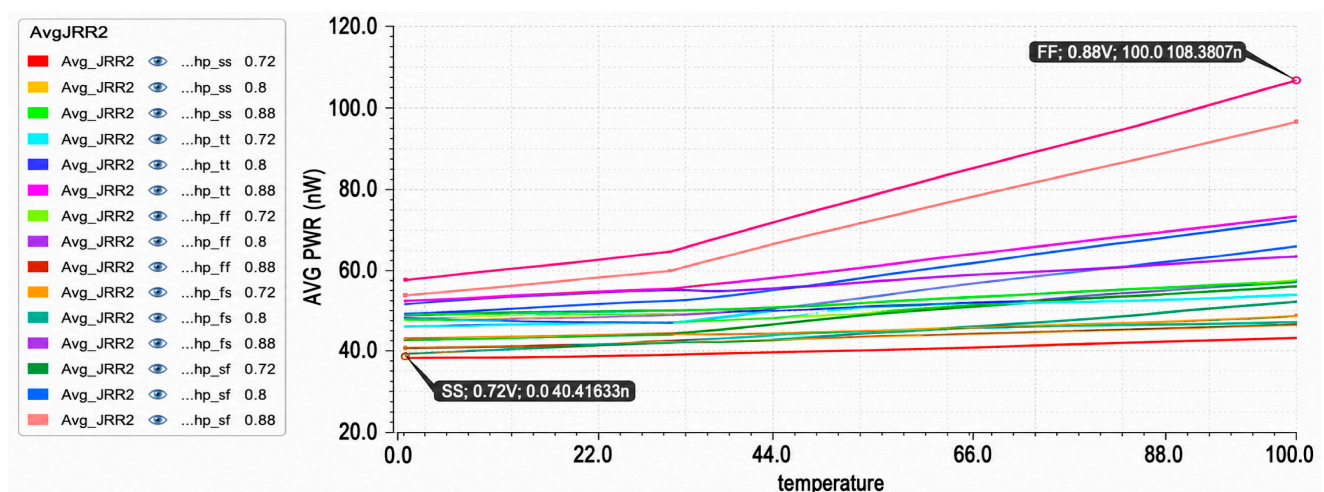


Figure 25. Average Power Consumption of the Post-layout JRR2 Comparator Under 45 PVT corner simulations.

Table 9 compares the post-layout average power consumption of the Shin, Paik, JRR1, and proposed JRR2 comparators under identical PVT conditions. Despite the additional parasitic effects introduced during layout extraction, the proposed JRR2 comparator continues to exhibit the lowest maximum and minimum average power consumption among all evaluated architectures. These results confirm that the proposed comparator preserves its energy-efficient characteristics after layout extraction while maintaining reliable operation across all evaluated PVT corners. Consequently, the proposed comparator remains well suited for ultra-low-power SAR ADC applications requiring robust operation under wide PVT variations.

Table 9. Comparison of Average Power Consumption under Post-layout PVT Simulations.

Comparator Configuration	Shin	Paik	JRR1	JRR2
Max. Average Power $V_{DD} = 0.88\text{ V}$; Temp. = $100\text{ }^{\circ}\text{C}$; Process = FF	1.5 μW	1.51 μW	114.04 nW	108.38 nW
Min. Average Power $V_{DD} = 0.72\text{ V}$; Temp. = $0\text{ }^{\circ}\text{C}$; Process = SS	131.15 nW	90.62 nW	47.65 nW	40.42 nW

4.6. Kickback Noise Analysis

Kickback noise is one of the critical limitations in dynamic comparator design, particularly for low-voltage SAR ADC applications where small differential input signals must be accurately resolved. During comparator operation, rapid voltage transitions in the regenerative latch may couple through parasitic capacitances and introduce unwanted disturbances at the input and output nodes. These disturbances can degrade decision accuracy, increase regeneration delay, and potentially lead to metastability under adverse operating conditions. Therefore, in addition to delay and power-performance evaluation, the kickback-noise characteristics of the proposed JRR2 comparator are investigated under both nominal and PVT operating conditions. The objective is to evaluate the effectiveness of the proposed threshold-controlled latch activation mechanism in suppressing regenerative disturbances while maintaining robust operation across wide environmental and manufacturing variations.

4.6.1. Nominal Kickback Noise Comparison

Kickback noise is an important performance parameter in dynamic comparators because the rapid voltage transitions occurring during latch regeneration can introduce unwanted disturbances to the input and output nodes through parasitic capacitive coupling. These disturbances may affect the accuracy of the comparator decision and degrade the overall performance of SAR ADCs. Comparator-induced kickback noise and decision errors may also contribute to ADC non-linearity by perturbing the sampled input voltage, particularly during low-level signal conversion. This relationship has been discussed in recent studies on SAR ADC linearity [31]. In double-tail dynamic comparators, the isolation between the dynamic amplifier stage and the regenerative latch helps reduce kickback noise. However, under low-voltage operation, kickback noise remains a critical concern due to the increased sensitivity of the regenerative process to parasitic capacitances and transistor switching activity. To mitigate kickback noise, the input differential pair transistors (M1 and M2) of the proposed JRR2 comparator were designed to operate in the weak-inversion region with a transistor size of $W/L = 8\text{ }\mu\text{m}/180\text{ nm}$, maximizing the g_m/I_D ratio while minimizing the disturbance coupled through the parasitic capacitances.

Furthermore, the threshold-controlled latch activation mechanism delays regeneration until sufficient differential gain is established by the dynamic amplifier stage, thereby reducing regenerative disturbances and improving noise immunity.

Figure 26 compares the kickback-noise characteristics of the Shin, Paik, JRR1, and proposed JRR2 comparators during the regeneration phase under nominal operating conditions (TT process corner, $V_{DD} = 0.8$ V, $T = 27$ °C, and $\Delta V_{in} = 800$ mV). The kickback-noise amplitude observed at the OOUTP node was 66.03 mVpp for the JRR2 comparator, compared with 82.42 mVpp, 104.04 mVpp, and 115.63 mVpp for the Shin, Paik, and JRR1 comparators, respectively. These results correspond to kickback-noise reductions of approximately 20%, 37%, and 43% relative to the Shin, Paik, and JRR1 architectures. The significant reduction in kickback noise confirms the effectiveness of the proposed threshold-controlled latch activation mechanism in suppressing regenerative disturbances during latch regeneration.

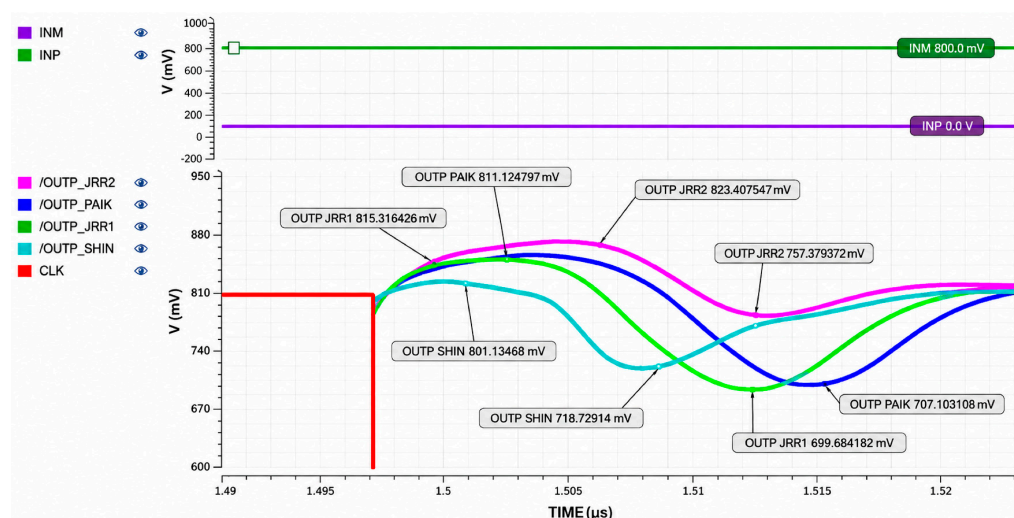


Figure 26. Comparison of Kickback Noise During the Regeneration Delay Under Nominal Operating Conditions.

4.6.2. Kickback Noise Performance Under 45 PVT Corner Simulation

Although the nominal simulation results demonstrate the effectiveness of the proposed JRR2 architecture in reducing kickback noise, it is also necessary to evaluate its robustness under PVT variations. During the regeneration process, rapid voltage transitions at the latch nodes may couple through parasitic capacitances and introduce disturbances at the signal nodes. Excessive kickback noise can increase decision uncertainty, prolong regeneration time, and potentially lead to incorrect comparator decisions. Figure 27 illustrates the kickback-noise behaviour of the proposed JRR2 comparator during the regeneration phase across all 45 PVT corners. The results show that the transient output disturbance remains bound under all operating conditions evaluated.

The maximum transient voltage excursion associated with kickback noise was observed at the FF process corner with $V_{DD} = 0.88$ V and $T = 100$ °C, producing an output level of 906.39 mV, while the minimum excursion occurred at the FF process corner with $V_{DD} = 0.72$ V and $T = 100$ °C, resulting in an output level of 708.69 mV. Despite the wide variation in PVT conditions, the comparator maintained stable regeneration characteristics without functional failure. These results indicate that the proposed threshold-controlled latch activation mechanism not only reduces kickback noise under nominal operating conditions but also maintains stable operation across a wide range of PVT variations.

Table 10 summarizes the maximum and minimum output-voltage excursions observed during the kickback-noise analysis across the evaluated PVT corners. The proposed JRR2 comparator exhibits the lowest regeneration noise of 197.7 mVpp, compared with

275.45 mVpp, 209.11 mVpp, and 328.31 mVpp for the Shin, Paik, and JRR1 comparators, respectively. The reduced noise level confirms the effectiveness of the threshold-controlled latch activation mechanism in suppressing regenerative disturbances. Furthermore, the absence of functional failures across all evaluated PVT corners demonstrates that the proposed JRR2 architecture maintains robust operation while achieving improved immunity to kickback-induced effects under wide PVT variations. The JRR2 comparator achieved the highest minimum output voltage among all evaluated architectures under worst-case operating conditions, indicating improved tolerance to kickback-induced disturbances.

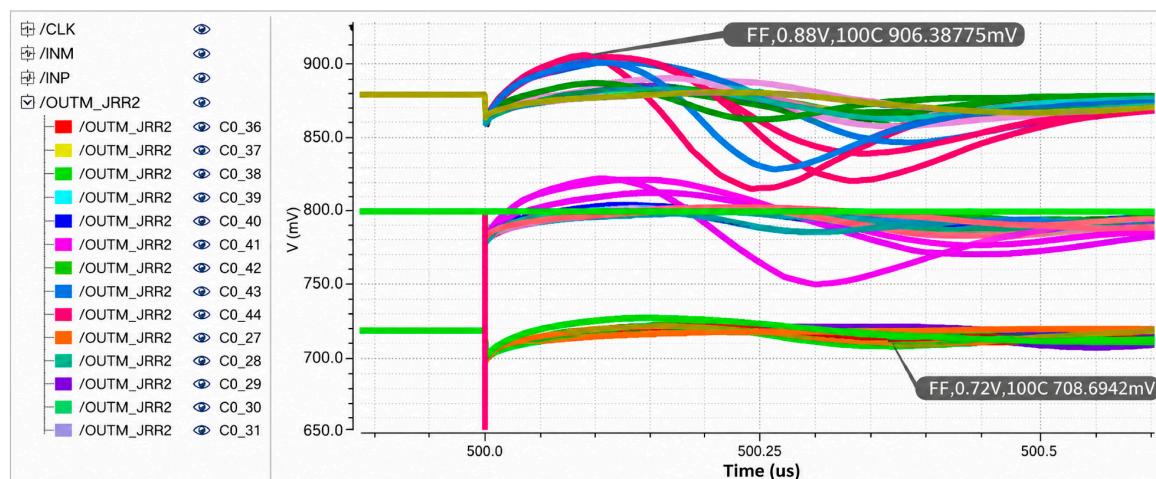


Figure 27. Kickback Noise During the Regeneration Delay of the JRR2 Comparator Under 45 PVT Corner Simulations.

Table 10. Kickback noise comparison in schematic PVT simulation.

Comparator Input Setup	SHIN	PAIK	JRR1	JRR2
Regeneration Phase $\Delta V_{in} = 800 \text{ mV}$ $V_{DD} = 0.88 \text{ V}$	(FF; 30 °C) 882.14 mV	(FF; 100 °C) 891.27 mV	(FF; 100 °C) 897.53 mV	(FF; 100 °C) 906.39 mV
Regeneration Phase $\Delta V_{in} = 800 \text{ mV}$ $V_{DD} = 0.72 \text{ V}$	(FS; 100 °C) 606.69 mV	(FS; 100 °C) 683.16 mV	(FS; 30 °C) 569.22 mV	(FF; 100 °C) 708.69 mV
Regeneration Noise (Vp-p)	275.45 mV	209.11 mV	328.31 mV	197.7 mV

5. Performance Comparison with State-of-the-Art Dynamic Comparators

To further evaluate the effectiveness of the proposed JRR2 comparator, a comparative assessment was conducted against representative low-voltage dynamic comparator architectures reported in the literature. The selected designs were chosen based on their relevance to low-power SAR ADC applications, with emphasis on energy efficiency, low-voltage operation, and robustness against process-induced performance variations. The comparison includes both energy-oriented and robustness-oriented comparator architectures to provide a comprehensive perspective on the performance characteristics of the proposed design relative to existing solutions.

As summarized in Table 11, the proposed JRR2 comparator demonstrates competitive energy efficiency while operating at a low supply voltage of 0.8 V in a mature 180 nm CMOS technology. Despite the larger technology node, the proposed comparator achieves an energy-per-comparison of 20.7 fJ/comparison-step, which is lower than that of the conventional double-tail comparator [24] and remains competitive with comparator ar-

chitectures implemented in more advanced 65 nm CMOS technologies [17,18,30]. The improved energy efficiency is primarily attributed to the proposed threshold-controlled latch activation mechanism, which minimizes unnecessary regenerative switching activity during the comparison process. In addition to competitive energy efficiency, comprehensive robustness verification represents one of the primary contributions of this work. Among the compared designs, only De La Fuente-Cortes et al. [18] reported robustness verification using 15 process–temperature (PT) corners. In contrast, the proposed comparator extends the verification framework to 45 Process–Voltage–Temperature (PVT) corners using the proposed Input Test Pattern (ITP)-based validation methodology, thereby providing three times the robustness verification coverage while simultaneously accounting for process, supply-voltage, and temperature variations. This comprehensive validation framework provides stronger evidence that the proposed comparator can maintain reliable functionality after fabrication under realistic manufacturing and environmental variations. Unlike previous studies that primarily focused on nominal performance or limited process–temperature verification, the proposed validation framework demonstrates reliable comparator operation under simultaneous process, voltage, and temperature variations, thereby providing a more comprehensive assessment of circuit robustness. Consequently, the proposed JRR2 comparator provides an effective balance between energy efficiency, low-voltage operation, and PVT robustness, making it a promising solution for differential low-power SAR ADC applications.

Table 11. Comparison of Representative Low-Voltage Dynamic Comparator Architectures.

Parameter	[24]	[18]	[30]	[17]	This Work (JRR2)
Comparator Type	Double-Tail Dynamic	PT-Robust	Dynamic Bias	Modified Double-Tail	Threshold-Controlled Latch
Technology	180 nm	65 nm	65 nm	65 nm	180 nm
VDD	0.8 V	1.2 V	1.2 V	1.0 V	0.8 V
Power Consumption	576 nW	375.6 μ W	0.75 μ W	4.8 μ W	41.4 nW
Energy per comparison	240 fJ/Com.	18,780 fJ/Com.	30 fJ/Com.	192 fJ/Com.	20.7 fJ/Com.
PVT Robustness Verification	N/R	15 PT Corners	N/R	N/R	45 PVT Corners (ITP)

Notes: N/R = Not Reported.

6. Conclusions

This paper presented a PVT-robust 0.8 V subthreshold double-tail dynamic comparator for differential 10-bit SAR ADC applications. The proposed JRR2 architecture incorporates a threshold-controlled latch activation mechanism that delays latch regeneration until sufficient differential voltage amplification is established by the dynamic amplifier stage, thereby suppressing premature regeneration, reducing kickback-induced disturbances, and improving decision stability under low-voltage operation. To comprehensively evaluate comparator robustness under manufacturing and environmental variations, a dedicated ITP-based validation methodology was developed and applied across 45 PVT corners comprising TT, SS, FF, FS, and SF process conditions, $\pm 10\%$ supply-voltage variation, and temperatures ranging from 0 °C to 100 °C. The proposed comparator successfully resolved a minimum differential input voltage of 0.8 mV while achieving a nominal post-layout regeneration delay of 327 ps, an average power consumption of 41.4 nW, and an energy efficiency of 20.7 fJ/comparison-step. Under

the worst-case operating conditions, regeneration delays of 29 ns and 105 ns, together with corresponding power consumptions of 68 nW and 108.38 nW, were obtained from schematic and post-layout simulations, respectively. Furthermore, the proposed architecture achieved a peak-to-peak kickback noise of 197.7 mV and successfully passed all 45 post-layout PVT corner simulations, confirming reliable functionality under wide process, voltage, and temperature variations. Compared with representative low-voltage dynamic comparators [17,18,24,30], the proposed JRR2 comparator demonstrates competitive energy efficiency, achieving an energy-per-comparison of 20.7 fJ/comparison-step while operating at a low supply voltage of 0.8 V in a mature 180 nm CMOS technology. More importantly, the proposed ITP-based validation methodology extends robustness verification from 15 process–temperature (PT) corners reported in [18] to 45 Process–Voltage–Temperature (PVT) corners, thereby providing three times the robustness verification coverage. Collectively, the presented results validate both the proposed threshold-controlled latch activation mechanism and the ITP-based validation methodology as effective approaches for achieving reliable, energy-efficient, and PVT-robust comparator operation. Overall, the proposed JRR2 comparator offers a practical and energy-efficient solution for ultra-low-power differential SAR ADCs requiring reliable operation under wide manufacturing and environmental variations. Future work may include Monte Carlo-based mismatch analysis to investigate the statistical impact of local device variations and provide further insight into comparator performance distributions.

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