A fault syndromes simulator for random access memories

Abstract

Testing and diagnosis techniques play a key role in the advance of semiconductor memory technology. The challenge of failure detection has created intensive investigation on efficient testing and diagnosis algorithm for better fault coverage and diagnostic resolution. At present, the March test algorithm is used to detect and diagnose all faults related to Random Access Memories. This algorithm also allows the faults to be located and identified. However, the test and diagnosis process is mainly done manually. Due to this, a systematic approach for developing and evaluating memory test algorithm is required. This work is focused on incorporating the March based test algorithm using a software simulator tool for implementing a fast and systematic memory testing algorithm. The simulator allows a user through a GUI to select a March based test algorithm depending on the desired fault coverage and diagnostic resolution. Experimental results show that using the simulator for testing is more efficient than that of the traditional testing algorithm. This new simulator makes it possible for a detailed list of coupling faults and stuck-at faults covered by each algorithm and its percentage to be displayed after a set of test algorithms has been chosen. The percentage of diagnostic resolution is also displayed. This proves that the simulator reduces the trade-off between test time, fault coverage and diagnostic resolution. Moreover, the chosen algorithm can be applied to incorporate with memory built-in self-test and diagnosis, to have a better fault coverage and diagnostic resolution. Universities and industry involved in memory Built-in-Self test, Built-in-Self repair and Built-in-Self diagnose will benefit by saving a few years on finding an efficient algorithm to be implemented in their designs.

Keyword: Testing; Diagnosis; Coupling faults; Stuck-at faults March Test Algorithm; Built-In Self-Test (BIST) Built-in Self-Diagnosis (BISD); Automated march-based test algorithm; SRAM