Scan Shift Power Evaluation of ISCAS89 Benchmark Circuits

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***Abstract*— Scan testing is one of the Design for Testability (DFT) techniques that is widely being used to detect the emerging manufacturing defects in nanometer process technology. However, due to the advancement in System-on-Chip (SoC), over hundred million of logic gates have been implemented in a design resulting in high power dissipation and it has been revealed that power dissipation during scan testing could achieve three times higher than during normal operation due to the switching activity. Thus, the aim of this paper is to investigate the number of scan chains and Automatic Test Pattern Generation (ATPG) X-filling method in reducing the switching power and switching activity. In this work, 12 ISCAS89 benchmark circuits are used to run the scan test by using DFT Compiler and TetraMAX ATPG from Synopsys. Single scan chain up to 20 scan chains is implemented during scan chain insertion and 4 distinct ATPG X-filling methods—random filling, 0-filling, 1-filling and adjacent filling is applied. The switching power and switching activity for each iteration is evaluated to find the optimum number of scan chains and the best ATPG X-filling for each circuit. The simulation results show that out of 12 circuits, 5 of them exhibit preference towards single-digit number of scan chains to achieve optimal switching power performance and the decrement of switching power is ranged from 0.06% to 7.18% compared to single scan chain. Meanwhile, 7 out of 12 circuits gravitate towards 0-filling in reducing switching activity. The decrement of switching activity ranged from 4.23% to 60.63%.**

***Index Terms*— Design for Testability, scan test, shift power.**

I. Introduction

Advance development in System-on-Chip (SoC) requires evolution of integrated circuit's (IC) process technology. The current trend of nanometer process technology demands the design of a device to become more complex with application over millions of transistors that results in increasing test complexities and more prone to manufacturing defects.

Other than manufacturing defects, another major issue in SoC is excessive power dissipation especially during test mode. One of the examples of excessive power dissipation is power obtained during parallel testing that is being carried out to reduce test application time. In a very complex design of SoC, there will be a tremendous increment number of scan flip flop (SFF). A high number of SFF in a scan chain will result in longer test time [1] and lead to increment of test cost [2]. In order to reduce the test time, a very long scan chain can be divided into several scan chains [3] that will run in parallel testing. However, choosing an optimum number of scan chains in a design is necessary because parallel testing will lead to high power dissipation [4]. Additionally, during test pattern generation which is one of essential part for scan testing, will further increase the power consumption through switching activity happened between the different bits. Previous work that have established concluded that switching power is one of the highest contribution of power distribution due to the rigorous switching activities [5-6] and it is observed as major drawback in scan testing [7]. Even though the power dissipation during scan test is known to be higher up to three times compared to during normal operation [8], the application of scan test during design process is essential to minimize manufacturing defects.

Several studies have been conducted on scan tests such as scan reordering, scan partitioning, scan stitching and modification on scan architecture to find the best method to reduce the power dissipation. In [9-16], the scan reordering is simulated with other techniques to obtain minimum power dissipation. Hamming distances between scan cells is calculated and the Traveling Salesman Problem (TSP) is employed in [9] in order to find the optimal scan sequence. In [10] the scan chain is reordered by utilizing the greedy algorithm with adjacent filling while [11] introduced reordering technique by considering the response correlation (RORC) and both pattern and response (ROBPR) to achieve low power design. [12] considered the bit pattern and employed the weight hamming distance (WHD) to reorder the scan chain. [13-14] did the scan reordering by focusing on the care bit density to reduce the transition count, [15] reordered the scan chain by limiting the range based on x-filling partitioning and calculated statistic value filling test pattern and lastly [16] performed scan reordering by calculating distance matrix between scan cells and implemented scan correlation clustering.

For scan cell partitioning, [17] partitioned the scan chains into segments and applied the separate clocks for each partition. In [18], multiplexers are placed between the partitions to allow the bypass of non-active segments during scan operation. Meanwhile, [11][19] partitioned the scan chain into equal segments and implemented a modified Ant Colony Optimization (ACO) algorithm to reorder the test vectors. Other than that, [20] implemented a scan stitching method by optimizing the flip flop and [21] stitched the scan chain with the similar logic weight calculated using weight-based segmentation. In [22] scan stitching is also applied by positioning the higher scan influence flip flop at the front of the scan chain and the lower scan influence flip flop at the end of the scan chain, then during test pattern generation, adjacent filling is utilized. [23] introduced a new scan cell routing algorithm by exploiting tri-state data and decoder during test compression step and completely exclude X-filling flow. Other than that, modifi-

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cation on the scan architecture was done by several researchers to produce a low power design. [24] introduced low-power Illinois scan architecture that added multiplexer to a splitted scan chain, [5] introduced scan architecture by disabling the second flip flop in the basic scan cell, [25] innovated single master latch and separate functional slave latch, [26] introduced an enhancement to California scan architecture by adding XOR gates between scan flip flop and [6] implemented XOR gates with buffer and inverter between flip flops in the basic scan architecture that can result decrement of power consumption. Meanwhile, [27] added secondary latch in the design to bypass the test vector of the combinational circuits existed between the SFF and [28] applied scan insertion directly during designing the Register Transfer Level (RTL) which can utilized the existing MUX in the circuit.

Automatic Test Pattern Generation (ATPG) generates test patterns with minimum pattern count and test application time. Test patterns with high toggle rate will also cause higher switching activity in test mode compared to normal mode. Many techniques have been studied to reduce the power dissipation such as adjustments that are made during test pattern generation. [29-30] introduced the concept of test pattern reordering. [29] reordered the test pattern by minimizing the transition density through an improved greedy algorithm while [30] reordered them based on the minimum Hamming distance between test patterns. Besides that, alteration of X-filling method is also an effective way to reduce the switching activity, hence, will result in lower power dissipation by identifying any don't care bits and assign specific value 0 or 1 to them [7]. Another advantage of the X-filling method is it does not require any modification to the circuit; thus, it does not result in area overhead [8]. [31] has extended the adjacent filling and constraining specific scan cell to a value to develop Bounded Adjacent Fill (BA-fill). [32] implemented fan-out-aware modification of adjacent fill by identifying the maximum fan out values and [33] generated the test pattern with MT-filling and determine the lowest transition count by calculating Weighted Transition Metric (WTM) to reduce the shift power. Besides, in [4][34-35], use multiple X-filling method strategies to reduce the switching activity. [34] applied random filling, 0-filling, 1-filling and adjacent filling during test pattern generation and eliminated the redundant patterns. The optimal test pattern is then selected by calculating using Weighted Switching activity (WSA). [35] also implemented multiple X-filling methods to identify any bits that have no impact to the final output, while in [4] the application of multiple X-filling method will be based on the logic dominance in the design such as 0-filling will be applied to AND dominance and 1-filling is applied to OR dominant. Logic dominance concept also used during designing five input circuits in [36] which are AND-OR-Inverter, NAND and NOR to prove that certain dominance can produced high switching power.

In this paper, number of scan chains and Automatic Test Pattern Generation (ATPG) X-filling are being studied on 12 ISCAS89 benchmark circuits. The switching power obtained by each circuit is being evaluated and an optimal number of scan chains and X-filling method for each circuit are investigated. The rest of the paper is organized as follows. Section II is about the methodology that will focus on the parameters involved to get the optimum number of scan chains and X-filling method. Section III is the discussion on the switching power and switching activity performance obtained for each circuit. The conclusion on this paper is presented in Section IV.

II. METHODOLOGY

Number of scan chain and X-filling method during test pattern generation are being studied on 12 ISCAS89 benchmark circuits encompass s298, s820, s953, s1423, s1494, s5378, s9234, s13207, s15850, s35932, s38417, and s38584 with clock frequency 16MHz. The designs being implemented using Synopsys DFT Compiler and TetraMAX ATPG targeted at 180 nm CMOS technology. Table I shows the ISCAS89 benchmark circuits selected for this work. These 12 benchmark circuits are being chosen randomly based on the number of D-flip flop (DFF) in the design. Before choosing specific circuits for this work, all ISCAS89 circuits are being divided into few categories and 2 circuits that meet requirement from each categories are being selected. The categories are:

1. Circuit with number of DFF more than 1.
2. Circuit with number of DFF more than 5.
3. Circuit with number of DFF more than 10.
4. Circuit with number of DFF more than 50.
5. Circuit with number of DFF more than 100.
6. Circuit with number of DFF more than 500.
7. Circuit with number of DFF more than 1000.
8. Circuit with number of DFF more than 1500.

During the first phase, the 12 ISCAS89 benchmark circuits are being simulated several times with a different number of scan chains which are 1, 2, 4, 6, 8, 10, 12, 14, 16, 18, and 20 and conventional X-filling test pattern which is random filling is employed during test pattern generation. Random filling is where the don't care bits in the test pattern is being replaced randomly with 0 or 1. During this phase, three parameters which are switching power, number of test pattern generation and percentage of test coverage are being evaluated to find an optimal number of scan chains for each design that can result in low switching power, low test pattern generation and high test coverage.

Table I. Circuit characteristics.

Circuit	# of DFF	# of primary input	# of primary output	# of and/or/not gates
s820	5	18	19	289
s1494	6	8	19	647
s298	14	3	6	119
s953	29	16	23	395
s1423	74	17	5	657
s5378	179	35	49	2779
s9234	211	19	22	5597
s15850	534	14	87	9772
s13207	638	31	121	7951
s38584	1426	12	278	19253
s38417	1636	28	106	22179
s35932	1728	35	320	16065

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Meanwhile, in the second phase, the 12 ISCAS89 benchmark circuits with the optimal scan chain are being simulated several times with multiple X-filling test pattern generation which are random filling, 0-filling, 1-filling and adjacent filling. For 0-filling, the don't care bits are replaced with 0, 1-filling replaced with 1 and adjacent filing the don't care bits are replaced by the most recent care bit in the pattern. During this phase, two parameters which are switching activities and number of test pattern generation are evaluated to determine the best X-filling method that can produce low power patterns. The ideal X-filling method is selected based on low values for both parameters. The default fault model adopted is the stuck-at-fault model, specifically focusing on stuck-at-faults for serial and parallel test.

Power dissipation in an IC comprises dynamic power ($P_{dynamic}$) and static power (P_{static}). Dynamic power is the power that dissipates when the circuit is active and it consists of switching power and internal power. Switching power is dissipated during the charging and discharging activities of the load capacitance. This charging and discharging of load capacitance exists when there is a logic transition. Hence, switching power [36] will increase if the frequency of logic transition increases and is given by the equation:

$$P_{switching} = ½ \cdot C_L \cdot V_{dd}^2 \cdot N.f \quad (1)$$

where C_L is load capacitance, V_{dd} is supply voltage, N is switching activity per second as shown in (1). Internal power is dissipated within the boundary of the cell. In the most library cell, internal power occurred mostly due to the existence of short circuit current that dissipated between P and N of transistors of the cell during logic transition as shown in equation:

$$P_{short\_circuit} = I_{sc} \cdot V_{dd} \cdot f \quad (2)$$

where I_{sc} is the short circuit current as shown in (2), V_{dd} is supply voltage and f is switching frequency [4]. Transition of logic (which also known as switching activity) from bit 1 to 0 and vice versa and test power is directly related to the dynamic power and it is calculated in equation

$$P_{dynamic} = P_{switching} + P_{short\ circuit} \quad (3)$$

Static power is the power dissipated when the transistor is not switching either when it is static or inactive. Large percentage of static power is contributed by sub-threshold leakage current and from leakage current between diffusion layer and substrate. This is the reason static power is also known as leakage power. The total of power dissipation [36] is calculated as in (4):

$$P_{total} = P_{dynamic} + P_{static} \quad (4)$$

In this work, the switching power is dominating the total power dissipation in the circuits during scan test, hence the evaluation of the switching power will be carried out.

III. Result and Discussion

Table II presented the overview of switching power in various numbers of DFF in the circuit design before and after the scan chain insertion. The percentage of increment of switching power highlighted the impact of the scan chains on the power consumption.

Table II. Switching power before and after scan insertion.

Circuit	# of DFF	Switching power before scan insertion (μw)	Switching power after scan insertion (chain 1) (μw)	Increment of switching power before and after scan insertion (%)
s820	5	6.19	6.41	3.55
s1494	6	24.01	28.38	18.20
s298	14	6.81	6.82	0.15
s953	29	6.96	7.53	8.19
s1423	74	14.76	16.43	11.31
s5378	179	36.46	43.47	19.23
s9234	211	29.24	38.04	30.10
s15850	534	77.12	92.75	20.27
s13207	638	57.41	101.8	77.32
s38584	1426	572.6	633.8	10.69
s38417	1636	458.2	475.5	3.78
s35932	1728	361.1	380.5	5.37

The insertion of the scan chain resulted in increment of switching power for all circuit designs due to replacement of the D flip-flop with scan flip-flop during scan chain insertion. It is interesting to note that the increase in switching power is not consistent with the increase in the number of scan flip-flop.

In finding an optimal number of scan chains, there are other factors apart from switching power that need to be taken into consideration which are maintaining a minimal number of test patterns and obtaining high test coverage [37]. In order to meet these conditions, an extensive simulation was conducted on all 12 circuits in determining the optimum number of scan chains that can satisfy the criteria of low switching power, low number of test patterns generated and high-test coverage using conventional ATPG filling (random filling). The number of scan chains inserted ranges from 1 to 20 for 9 of the circuits. Note that from the 12 cir cuits, 3 circuits are selected with fewer DFF numbers which is less than 20, thus the maximum number of scan chains inserted is different.

Table III shows the reduction of switching power achieved by each circuit design after implementation of the optimal number of scan chains in comparison to the single scan chain which varies from 0.06% to 7.18%.

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Table III. Optimum number of scan chain.

Circuit	Single scan chain with conventional ATPG filling				Optimum scan chain with conventional ATPG filling					Decrement of switching power (%)
	# of scan cells per chain	# of test patterns	Test coverage (%)	Switching power (μw)	Optimum number of scan chain	# of scan cells per chain	# of test patterns	Test coverage (%)	Switching power (μw)	
s820	5	80	100	6.41	4	1 & 2	82	100	6.18	3.59
s1494	6	95	99.34	28.38	6	1	96	99.56	28.28	0.35
s298	14	24	100	6.82	14	1	24	100	6.33	7.18
s953	29	95	100	7.53	20	1 & 2	95	100	7.32	2.79
s1423	74	32	99.16	16.43	2	37	32	99.42	16.42	0.06
s5378	179	64	98.68	43.47	18	9 & 10	64	98.81	42.76	1.63
s9234	211	96	99.58	38.04	10	21 & 22	96	99.69	37.65	1.03
s15850	534	64	99.53	92.75	18	29 & 30	64	99.55	91.86	0.96
s13207	638	64	99.09	101.8	12	53 & 54	64	99.10	99.13	2.62
s38584	1426	64	98.90	633.8	16	89 & 90	64	98.92	632.1	0.27
s38417	1636	64	99.68	475.5	4	409	64	99.75	474.8	0.15
s35932	1728	19	100	380.5	4	432	18	100	363.1	4.57

In obtaining the optimal scan chain, this work will compare three parameters; switching power, number of test pattern generation and percentage of test coverage between multiple scan chains first to obtain a scan chain with low switching power, low number of test pattern generated and high test coverage. The chosen scan chain is then being compared with the reference design which is the single scan chain to see whether the chosen scan chain can get better performance especially in term of power. Table III shows that by applying the optimal number scan chains, it will be able to improve test coverage and minimize the power dissipation during scan test operations. It is also interesting to note that one scan chain in each design show low switching power but if there is a need to have more than 1 scan chain, for example to reduce the test time, finding the optimum number of scan chain is important.

The decrement of the switching power can be further reduced during test pattern generation. In this work, the X-filling method is being evaluated by applying 4 distinct methods which are conventional X-filling method (random filling), 0-filling, 1-filling and adjacent filling. Table IV shows the overview of the expected outcome when implementing X-filling method.

Table IV. Expected outcome for each X-filling method.

Example data	0XXX1X0XX0X1X	
X-filling method	Expected outcome	Explanation
Random filling	0101110010110	Don't care bits are randomly replaced with 0 and 1
0-filling	0000100000010	Don't care bits are replaced with 0
1-filling	0111110110111	Don't care bits are replaced with 1
Adjacent filling	0000110000011	Don't care bits are replaced with most recent care bits

The tool will replace the don't care bits in the input data to either 0 or 1 depending on X-filling method assigned. This care bits will further shifted out to output pins. Fig. 1 – Fig. 4 shows the example of shift transition of the first ten bits of test pattern generated of different X-filling method which are random filling, 0-filling, 1-filling and adjacent filling method.

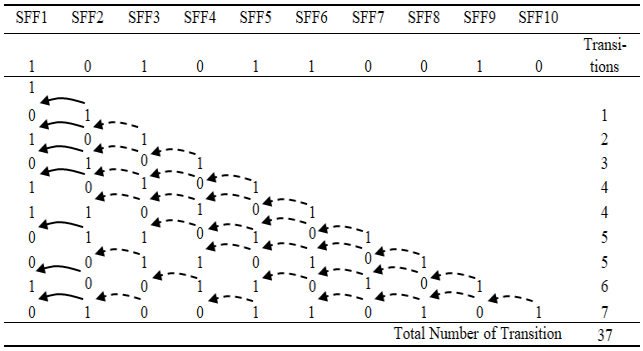

Fig.1 Shift transition for random filling method

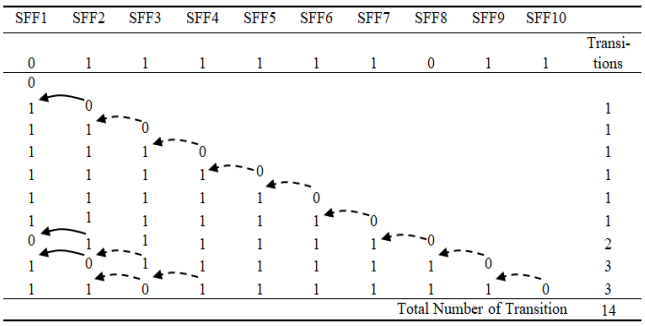

Fig.2 Shift transition for 0-filling method

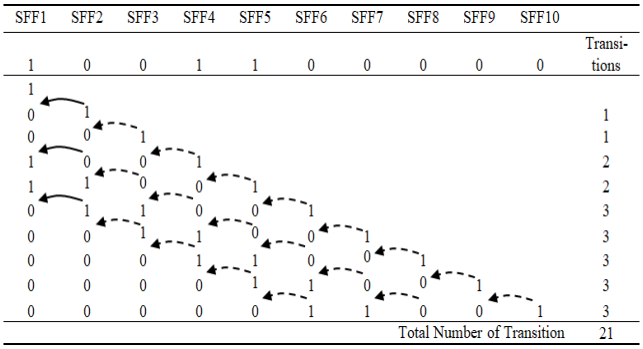

Fig.3 Shift transition for 1-filling method

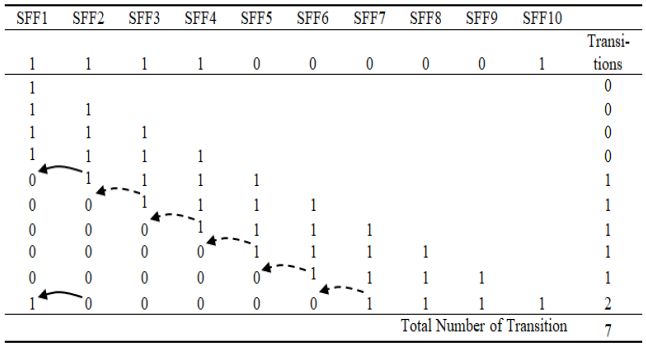

Fig.4 Shift transition for adjacent filling method

Theoretically, the conventional ATPG which is the random filling will require highest number of switching activity while adjacent filling will require lowest switching activity due to their transition concept as shown in Fig. 1 – Fig. 4. However, [4][20][33][36] found that the logic dominance in a circuit and bit location of the test pattern will also affect the switching activity, thus, depending on the design, any X-filling method can be the suitable method to produce low power dissipation.

Table V presented the best X-filling method that can obtain a lower number of switching activities in comparison to random filling. Since switching power is obtained by the toggling process of the bits during switching activity, thus, lower switching activity indicates lower switching power.

Even though some of the circuits with applied best X-filling method obtain lower test coverage compared to conventional ATPG method, the number of switching activity are reduced for all circuit ranging from 4.23% to 60.63%. Table VI shows the summary of the two methods in the scan test that are used in this work in achieving low test power design which are determining the optimum scan chain and evaluating the best X-filling method.

From the Table VI, it illustrates that the optimum number of scan chains and the best X-filling method are varied across the 12 ISCAS89 benchmark circuits evaluated in this work. 5 from the 12 circuit designs prefers a single-digit number of scan chains to achieve optimal function. Out of these 12 circuits, 7 of them favor 0-filling method in reducing switching power. 4 of them prefer adjacent filling and remaining 1 circuit chose 1-filling method as the best X-filling method in minimizing power dissipation during scan test.

This variation underscores the fact that design exploration is a time-intensive process. Identifying the optimal configuration for a particular design requires thorough analysis and testing across various parameters, including scan chain numbers and X-filling methods. The need for tailoring approaches to specific circuit designs means that no single solution fits all, and engineers must dedicate considerable time to evaluate and refine these configurations to meet the desired performance and power objectives

Table V. Switching activity with best X-filling method.

Circuit	Conventional ATPG (Random filling)			Best X-filling method				Decrement number of switching activity (%)
	# of test pattern	Test coverage (%)	# of switching activity	Best X-filling method	# of test pattern	Test coverage (%)	# of switching activity	
s820	82	100	177.5	0-filling	81	100	170	4.23
s1494	96	99.56	287	1-filling	95	99.71	271	5.57
s298	24	100	161	0-filling	23	100	116	27.95
s953	95	100	949	0-filling	89	99.54	413	56.48
s1423	32	99.42	1,059.78	*Adj filling	32	99.42	702.94	33.67
s5378	64	98.81	5,209.3	*Adj filling	64	98.56	3,180.4	38.95
s9234	96	99.69	9,968.27	0-filling	95	99.58	6,061.29	39.19
s15850	64	99.55	16,394.8	0-filling	64	99.33	8,041.75	50.95
s13207	64	99.10	20,287.3	0-filling	64	98.92	8,333.7	58.92
s38584	64	98.92	45,411.1	0-filling	64	99	24,504.3	46.04
s38417	64	99.75	48,052.2	*Adj filling	64	99.64	21,904.8	54.41
s35932	18	100	12,261.6	*Adj filling	18	100	4,826.99	60.63

*Adjacent filling

Table VI. Number of optimum scan chain and best X-filling method for 12 ISCAS89 benchmark circuits.

Circuit	Optimum number of scan chain	Best x-filling method
s820	4	0-filling
s1494	6	1-filling
s298	14	0-filling
s953	20	0-filling
s1423	2	Adjacent filling
s5378	18	Adjacent filling
s9234	10	0-filling
s15850	18	0-filling
s13207	12	0-filling
s38584	16	0-filling
s38417	4	Adjacent filling
s35932	4	Adjacent filling

IV. Conclusion

In this work, a scan-based DFT technique is applied to a variety of ISCAS89 benchmark circuits to obtain the optimization of test power during scan chain insertion and pattern generation. In order to determine the optimal number of scan chains, an evaluation on power dissipation, test pattern generations and test coverage is conducted. Besides, this work also explores distinct types of X-filling methods during test pattern generation, encompassing random filing, 0-filling, 1-filling and adjacent filling. The selection of the most ideal X-filling method is based on the analysis of switching activities and number of test pattern generation. The result obtained from the simulation has revealed that the optimal number of scan chains are varied across the diverse circuits of ISCAS89 benchmark circuits with the decrement of switching power ranging from 0.06% to 7.18%. The diversity of the circuit design also prefers different X-filling methods where 0-filling emerged as the preferred choice for 7 circuits, while adjacent filling is chosen for 4 circuits and 1-filling excelled for 1 circuit with decrement of switching activities ranging from 4.23% to 60.63%. This work successfully optimized the test power performance of the circuits involved by determining the optimal scan chain numbers and exploring the suitable X-filling method. Even though it is proven that optimal scan chains can reduce power performance, however, multiple scan chains will require many test pins during post silicon stage. Other than that, since switching activity will depend on the types of logic inside a circuit [4][36] and the location of the bit during test pattern generation [20][33], there is no guarantee one specific X-filling method is suitable filling method for all the circuit existed. Thus, the logic dominance and the bit location of a circuit need to be study first before implementing this method which might lengthen the scan testing process. Some improvement also can be applied in the future such as algorithm enhancement for X-filling method to further reduced the test power and enhanced test coverage. In-depth analysis on power dissipation also can be done to analyze different techniques for scan chain insertion and X-filling method to get deeper understanding of power-efficient DFT strategies. Other than that, leveraging on advanced algorithms and machine learning techniques can help automate the design space exploration process. These tools can intelligently traverse the vast number of potential configurations, identifying optimal solutions based on specified performance, power and area constraints. This reduces the time spent on manual exploration while ensuring thorough analysis.

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