



UNIVERSITI PUTRA MALAYSIA

**POWER AMPLIFIERS LINEARIZATION
BASED ON COMPLEX GAIN MEMORY PREDISTORTION**

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BASED ON COMPLEX GAIN MEMORY PREDISTORTION**

By

POORIA VARAHRAM

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in
Fulfilment of the Requirements for the Degree of Doctor of Philosophy

January 2010



DEDICATION

This thesis is dedicated to my lovely wife Somayeh who support me and help me to complete this thesis. She is everything in my life. I also dedicate this thesis to my parents and family who raised me and support me to continue my studying. Thank you for all the unconditional love, guidance, and support that you have always given me, helping me to succeed and the confidence that I am capable of doing anything I put my mind to.



Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of doctor of philosophy

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January 2010

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Faculty: Engineering

Power Amplifiers (PAs) are important components in communication systems and are nonlinear. The nonlinearity creates out of band distortion beyond the signal bandwidth, which interferes with adjacent channels. It also causes distortions within the signal bandwidth, which decreases the bit error rate at the receiver. Digital predistortion is one of the most cost effective ways among all linearization techniques to compensate for these nonlinearities.

In this thesis a novel technique for compensating memory effects and out of band distortions is proposed and is called Complex Gain Memory Predistortion (CGMP). The main advantage of the CGMP technique as compared to the memory polynomial technique is the ability of this technique to compensate all the memory effects inside the PA. Two structures of the CGMP technique are proposed. The CGMP technique is examined using two approaches, simulation and experiment. Power amplifiers are



modeled with memory polynomial technique to examine the effects of the memory that causes increment in Adjacent Channel Leakage Ratio (ACLR). To implement this method, the complex divider is required. This complex divider is then designed and implemented in Field Programmable Gate Array (FPGA) and combined with other parts to make the predistortion block. The CGMP is implemented in Virtex 5 FPGA and simulated using Xilinx blocks in Matlab. In the experimental approach the CGMP is examined with the actual power amplifier ZVE-8G from Mini Circuit. Finally the CGMP technique is compared with memory polynomial method and validated using a 1.9 GHz 60W LDMOS power amplifier that is designed in simulation and various signals such as 2-carrier WCDMA with 10 MHz carrier spacing and Mobile WiMAX with 10 MHz bandwidth. The simulations results showed between 25 to 30 dB improvement in ACLR and almost 5 dB improvement as compared to the memory polynomial method. The experimental results also show around 10 dB reduction in ACLR with applying QPSK signal with 1 MHz bandwidth. The improvement of 7 percent in Power Added Efficiency (PAE) is also achieved.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah doktor falsafah

**PELELURUSAN PENGUAT KUASA BERDASARKAN PRAHEROTAN
INGATAN GANDAAN KOMPLEKS**

Oleh

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Januari 2010

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Penguat Kuasa (PAs) merupakan komponen yang penting dalam sistem komunikasi dan ia tidak linear. Ketaklinearan ini menghasilkan herotan di luar kelebaran jalur isyarat. Ia juga menyebabkan herotan di dalam lebar jalur isyarat yang mengakibatkan kesalahan kadar bit pada penerima. Praherotan digital merupakan kaedah yang paling efektif dikalangan teknik pelinearan yang ada untuk mengatasi masalah ketaklinearan ini.

Dalam tesis ini, satu teknik novel untuk mengatasi masalah ingatan memori dan herotan di luar kelebaran jalur menggantikan kesan-kesan sedemikian dicadangkan. Ia dinamakan praherotan ingatan gandaan kompleks (CGMP). Kelebihan teknik CGMP ini dibandingkan dengan teknik memori polynomial adalah kebolehannya untuk menandingi semua kesan memori yang terdapat dalam PA. Oleh itu, dua struktur CGMP adalah dicadangkan.

Teknik CGMP ini diuji menggunakan teknik simulasi dan eksperimen. Penguat kuasa dimodelkan bersama teknik memori polinomial untuk menguji kesan ingatan yang menyebabkan peningkatan kepada kadar kebocoran saluran bersebelahan (ACLR). Untuk melaksanakan kaedah ini, pembahagi kompleks diperlukan. Ia direkabentuk dan di-hasilkan menggunakan tatasusunan get boleh program (FPGA) dan digabungkan bersama komponen lain untuk menghasilkan blok praherotan. Teknik CGMP dilaksanakan pada Virtex 5 FPGA dan disimulasi menggunakan blok Xilinx yang terdapat pada Matlab. Eksperimen CGMP ini diuji menggunakan penguat kuasa sebenar ZVE-8G daripada Mini Circuit. Seterusnya, teknik ini dibandingkan dengan teknik memori polinomial dan diuji menggunakan 1.9 GHz 60W LDMOS penguat kuasa dan pelbagai saluran seperti pembawa 2 WCDMA dengan pembawa jarak 10 MHz dan Mobile WiMAX dengan jalur lebar 10 MHz lebar jalur. Hasil simulasi menunjukkan peningkatan 25-30 dB dalam ACLR dan peningkatan hampir 5 dB jika dibandingkan dengan teknik memori polinomial. Hasil kajian ini juga menunjukkan pengurangan hampir 10 dB dalam ACLR dengan menggunakan 1 MHz lebar jalur saluran QPSK. Peningkatan sebanyak 7 peratus untuk kuasa tambahan (PAE) turut tercapai.

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TABLE OF CONTENTS

	Page
DEDICATION	ii
ABSTRACT	iii
ABSTRAK	v
ACKNOWLEDGEMENTS	vii
APPROVAL	viii
DECLARATION	x
LIST OF TABLES	xiv
LIST OF FIGURES	xv
LIST OF ABBREVIATIONS	xx
CHAPTER	
1 INTRODUCTION	1
1.1 Background	1
1.2 Problem Statement	3
1.3 Related Work	4
1.4 Research Methodology	7
1.5 Research Scope	9
1.6 Thesis Contribution	11
1.7 Thesis Organization	12
2 POWER AMPLIFIERS LINEARIZATION	14
2.1 Introduction	14
2.2 Power Amplifiers	14
2.2.1 Power Amplifier Characteristics and Nonlinear Effects	15
2.2.2 Power Amplifier Two Tone Test	20
2.2.3 Trade Off Between Linearity and Efficiency	
2.2.4 Class A	26
2.2.5 Class B	29
2.2.6 Class AB	30
2.2.7 Class F	31
2.3 Power Amplifier Memory Effects	31
2.3.1 Electrical Memory Effects	33
2.3.2 Electrothermal Memory Effects	33
2.4 Power Amplifiers Modelling	34
2.4.1 Modeling Memoryless Power Amplifiers	34
2.4.2 Power Amplifiers Model with Memory Effects	36
2.5 Power Amplifier Linearization Techniques	39
2.5.1 Feedback Linearization Technique	39
2.5.2 Linear Amplification with Nonlinear Components (LINC)	40
2.5.3 Feedforward Linearizers	42



2.5.4	Predistortion Linearizers	44
2.5.5	Digital Predistortion	45
2.5.6	Look-up Table Block	46
2.5.7	Complex Gain Multiplier	47
2.5.8	Adaptive Algorithm Block	48
2.6	Memory Polynomial Predistortion	49
2.7	Complex Gain Predistortion	52
2.8	Review of Literatures on Memory Effects in Digital Predistortion	55
2.9	Advantages and Dsiadvantages of the Linearization Techniques	57
2.10	Chapter Summary	58
3	DESIGN OF COMPLEX GAIN MEMORY PREDISTORTION	59
3.1	Introduction	59
3.2	Digital Predistortion Linearization Method	60
3.3	The Proposed Complex Gain Memory Predistortion	62
3.4	Advantages and Disadvantages of CGMP Method	71
3.5	Power Amplifier Simulations	72
3.6	Simulation results of applying the CGMP	79
3.7	Chapter Summary	93
4	HARDWARE IMPLEMENTATION	94
4.1	Introduction	94
4.2	Simulation with Xilinx Blocksets	94
4.2.1	System Generator	95
4.3	The Xilinx EDK	96
4.4	Field Programmable Gate Array (FPGA)	97
4.4.1	Description	98
4.4.2	Functional Description	99
4.5	CGMP Implementation	99
4.5.1	Complex Multiplier	100
4.5.2	Lookup tables (LUT)	101
4.6	Complex Divider Implementation	103
4.6.1	Complex valued division	103
4.6.2	Newton Raphson Division	105
4.6.3	Error Analysis	106
4.6.4	Initial Approximation Techniques	107
4.7	Hardware Structure of the complex divider	107
4.7.1	Divisor scaling	108
4.7.2	Newton Raphson Method	110
4.7.3	Postscaling of Division Values	110
4.8	Results of FPGA Implementation	116
4.9	Chapter Summary	122
5	EXPERIMENTAL RESULTS	123
5.1	Introduction	123
5.2	Experimental Setup	123
5.3	Experimental Results	130

5.4 Comparison between Simulation and Experimental Results	135
5.5 Chapter Summary	138
6 CONCLUSION AND SUGGESTIONS FOR FUTURE WORKS	139
6.1 Conclusions	139
6.1.1 Design the Complex Gain Memory Predistortion (CGMP) Technique	140
6.1.2 Design a New Complex Divider Block	140
6.2 Suggestions for Future Works	141
REFERENCES	143
APPENDICES	150
BIODATA OF STUDENT	188
LIST OF PUBLICATIONS	189



LIST OF TABLES

Table		Page
2.1:	Efficiency and linearity vs. PA classes of operation	26
2.2:	Comparison of linearization methods	49
2.3:	Review of Literature on Memory Effects in Digital Predistortion	56
3.1:	Comparison of two predistortion techniques for different PAs with 2 carrier WCDMA signal	86
4.1:	XC5VFX30T features	99
4.2:	Hardware resources of the CORDIC Divider	112
4.3:	Hardware resources of the Divider Implementation	112
4.4:	Hardware resources of the predistortion filter	115
5.1	Input Signal Parameters	124



LIST OF FIGURES

Figure		Page
1.1:	Study scheme showing the proposed work	7
1.2:	Flow chart of the research scope	9
2.1:	Power Amplifier Distortion Characteristics	16
2.2:	Compression and Intercept Points of PA	17
2.3:	AM-AM and AM-PM characteristics the distorted output signal	18
2.4:	Characteristic of the power amplifier	19
2.5:	Harmonic Distortion of the Two Tone Test	20
2.6:	Input and output spectra of a power amplifier	21
2.7:	Error Vector representation	23
2.8:	Power amplifier classes	24
2.9:	Circuit diagram of Class A, B, or C	28
2.10:	Voltage and Current waveform of a class A amplifier	28
2.11:	Voltage and Current waveform of a class B amplifier	30
2.12:	Voltage and Current waveform of a class AB amplifier	30
2.13:	Voltage and current waveforms for an ideal Class F	31
2.14:	Principle of distortion cancellation and its sensitivity to memory effects	32
2.15:	The AM-AM and AM-PM responses of a Class AB power amplifier	35
2.16:	Block Diagram of the Simple Feedback to Linearize Power Amplifiers	40
2.17:	LINC method to Linearize Power Amplifiers	41
2.18:	Constant Envelope Signals generation	42
2.19:	Feedforward general block diagram	43
2.20:	Block diagram of the predistortion linearization	44



2.21:	Block diagram of digital predistortion	46
2.22:	Complex Gain Multiplier Block	47
2.23:	The indirect learning architecture for the predistorter	50
2.24:	Flowchart of the memory polynomial predistortion	51
2.25:	Internal Blocks of Adaptive Predistortion	52
2.26:	Flowchart of the complex gain predistortion	54
3.1:	Adaptive digital predistortion block	61
3.2:	Cascade of predistortion and power amplifier	62
3.3:	Predistortion block with memory compensation (Case 1)	67
3.4:	Simplified predistortion block with memory compensation (Case 2)	68
3.5:	Flowchart of the Complex Gain Memory Predistortion (CGMP) method that proposed here	70
3.6:	Schematic of MRF1806 power amplifier	73
3.7a:	Input matching	73
3.7b:	Output matching	74
3.8:	S-parameters curves of MRF1806 power amplifier	74
3.9a:	The AM-AM characteristic of MRF1806 power amplifier	75
3.9b:	The AM-PM characteristic of MRF1806 power amplifier	75
3.10:	Flowchart of the power amplifier model with memory effects	76
3.11a:	AM-AM characteristics of the 1.9 GHz LDMOS	78
3.11a:	AM-PM characteristics of the 1.9 GHz LDMOS	78
3.12a:	AM-AM characteristics of the PA after applying CGMP method when the input back off is nearly 2 dB after 1 iteration	80
3.12b:	AM-AM characteristics of the PA after applying CGMP method when the input back off is nearly 2 dB after 5 iteration	80
3.13a:	AM-PM characteristics of the PA after applying predistortion	



	method when the input back off is nearly 2 dB after 1 iteration	81
3.13b:	AM-PM characteristics of the PA after applying predistortion method when the input back off is nearly 2 dB after 5 iteration	81
3.14:	Power amplifier input after applying predistortion function with 5 iterations	82
3.15:	Complex gain memory predistortion function after 5 iterations	83
3.16:	Error voltage of the power amplifier after 5 iterations	84
3.17:	Power Spectral Density (PSD) of the power amplifier with memory for different IBO with WiMAX signal	85
3.18:	Power spectral density for two different power amplifiers with 2 carrier WCDMA signal applied	87
3.19:	Comparison of the power spectral density (PSD) between memory polynomial predistorter and CGMP for 2 carrier WCDMA signal for power amplifier with MEMR=1	88
3.20:	Comparison of the power spectral density (PSD) between memory polynomial predistorter and gain predistortion for 2 carrier WCDMA signal for power amplifier with MEMR=0.45	89
3.21:	Comparison of the power spectral density (PSD) between memory polynomial predistorter and gain predistortion for power amplifier with MEMR=0.45 and Mobile WiMAX signal.	90
3.22:	Comparison of the power spectral density between memory polynomial predistorter and gain predistortion for power amplifier with MEMR=1 and Mobile WiMAX signal.	91
3.23:	Error Vector Magnitude of the power amplifiers with different memory effects for the CGMP technique.	92
3.24:	Error Vector Magnitude of the power amplifiers with different memory effects for the memory polynomial method.	92
4.1:	Flowchart of the system design flow using the Xilinx EDK	97
4.2:	The Virtex 5 FXT Evaluation Board	98
4.3:	Complex multiplier implementation with Xilinx blocks	101
4.4:	Single port RAM xilinx block	101
4.5:	The flowchart of the complex divider implementation	108



4.6:	Xilinx blocksets of the standard Input/dividend prescaling block	109
4.7:	Newton Raphson implementation with xilinx blocksets	110
4.8:	Complex divider block	111
4.9:	Complex divider implementation with Xilinx blocksets	111
4.10:	The error graph of the CORDIC divider for 4096 samples	113
4.11:	The error graph of the complex divider for 5 iterations Newton Raphson and 4096 samples	113
4.12:	CGMP block	114
4.13:	JTAG Co-simulation Block of the predistortion filter	115
4.14:	Comparison of PSD between simulation and implementation results	117
4.15:	Comparison of PSD between simulation and implementation results	117
4.16:	Predistortion filter Simulation with power amplifier	120
4.17:	Predistortion filter implementation with Xilinx blocksets	121
5.1:	Experimental Setup for linearization of PA using CGMP technique	126
5.2:	The photograph of the experimental setup	127
5.3:	Flowchart for experimental testing of the CGMP technique	129
5.4a:	AM-AM characteristics of the ZVE-8G PA	131
5.4b:	AM-PM characteristics of the ZVE-8G PA	131
5.5:	VSA Software Measurements Display for the ZVE-8G PA without applying CGMP	133
5.6:	VSA Software Measurements Display for the ZVE-8G PA with applying CGMP	133
5.7:	Power spectral density of the ZVE-8G power amplifier without CGMP	134
5.8:	Power spectral density of the ZVE-8G power amplifier with applying CGMP after 5 iterations	134



5.9:	Comparison of PSD for ZVE power amplifier	136
5.10:	Comparison of PSD for ZVE-8G power amplifier	136
5.11:	PAE of the ZVE-8G power amplifier with and without CGMP and with memory polynomial method	137
A.1:	Energy spectrum of a bandpass signal	151
A.2:	Schemes for converting between complex baseband and bandpass representations. Note that the LPF simply removes the double frequency term associated with the down conversion	153
A.3:	The complex envelope energy spectrum of the bandpass signal	155
C.1:	Input Voltage data samples before normalization for 1024 data samples	171
C.2:	Output Voltage data samples before normalization for 1024 data samples	171



LIST OF ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio
ACLR	Adjacent Channel Leakage Ratio
AM-AM	Amplitude Modulation to Amplitude Modulation
AM-PM	Amplitude Modulation to Phase Modulation
BB	Base Band
BER	Bit Error Rate
CDMA	Code Division Multiple Access
CGMP	Complex Gain Memory Predistortion
CORDIC	COordinate Rotation Digital Computer
DPD	Digital Predistortion
EDK	Embedded Development Kit
EVM	Error Vector Magnitude
FPGA	Filed Programmer Gate Array
GPIO	General Purpose Interface Bus
IBO	Input Power Back Off
IF	Intermediate Frequency
IMD	Inter Modulation Distortion
LINC	Linear amplification with Nonlinear Components
LTI	Linear Time Invariant
LUT	Look Up Table
MEMR	Memory Effect Modeling Ratio
OFDM	Orthogonal Frequency Division Multiplexing
OPBO	Output Power Back Off
PA	Power Amplifier



PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratios
PSD	Power Spectral Density
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RF	Radio Frequency
SCPI	Standard Command for Programmable Instruments
SER	Symbol Error Rate
VSA	Vector Signal Analyzer
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	Wireless Local Area Network



CHAPTER 1

INTRODUCTION

1.1 Background

Power Amplifiers (PAs) are necessary components in communication systems and they are nonlinear in a certain operation region. The nonlinearity generates spectral regrowth, which leads to Adjacent Channel Interference (ACI) and violations of the out of band emission. To reduce the nonlinearity, the power amplifier can be backed off to operate within the linear portion of its operating curve. However, transmission formats such as Wideband Code Division Multiple Access (WCDMA) and Orthogonal Frequency Division Multiplexing (OFDM), have high Peak to Average Power Ratios (PAPR), it means the large fluctuations in their signal envelopes. This means that the power amplifier needs to be backed off far from its saturation point, which results in very low efficiencies, typically less than 10% (Wright, 2002), more than 90% of the dc power is lost and turns into heat. With increasing the number of the base stations and then the number of power amplifiers improvement in efficiency of the power amplifier reduce the cost of the system. To improve the power amplifier efficiency without compromising its linearity, power amplifier linearization is essential.

Another important fact is with the increasing the number of users, greater amount of bandwidth is required. One of the effective ways to increase the bandwidth is to use diversity techniques, which have been applied in most of the 3G (Third Generation) standards specifications (Vuolvei, 2003). But, with each additional antenna, an additional transceiver is required which can significantly increase the system cost.

Another method is the Digital Predistortion (DP) technique. The DP technique overcomes the linearity problem of PAs, enabling the use of non-linear PAs that are cheaper, so reducing the cost of the overall system (Kenington, 2000). Digital predistortion among all linearization techniques is the one that is low cost and with high efficiency and also high flexibility. By applying digital predistortion which is implemented in baseband of the communication systems the nonlinearity of the power amplifier is reduced and it allows the use of high power amplifier with high efficiency in the systems.

Another important fact in studying PA is the memory effects that are the main issue of this research. The focus here is on the short term memory effects which cause the characteristics of PA to vary with time. This effect is more important where the high bandwidth signals are applied. The memory effects cause an increase in Adjacent Channel Leakage Ratio (ACLR) and also Error Vector Magnitude (EVM) which will be explained in Chapter 2. The other factor which might cause problem to the performance of the predistortion is the effect of the noise. Noise here can be result of the analog part such as DAC, mixer and so on which in this thesis are not considered, because the predistortion here is implemented in base band. The other noise source also can be from power amplifier which will be under memory effects and with the feedback that is in the adaptive predistortion that noise will be cancelled. In this thesis the linearization techniques of the power amplifiers mainly class AB are investigated, then digital predistortion technique is chosen as it is the most cost effective and most efficient among all the linearization techniques. The class AB power amplifier is chosen because of the more linearity of it as compare to other classes. A new technique has been developed, simulated and experimentally

measured to validate this new technique. Finally the simulation and experimental results are compared together.

1.2 Problem Statement

The main problem of this research is the out of band distortions or spectral regrowth that cause increment in ACLR. The reason that this happens is because of the nonlinearity of the power amplifier that should be reduced to overcome the loss of energy and also the adjacent channel interference.

The other problem is the power amplifier memory effects that cause the characteristics of power amplifier to change especially dynamic AM-AM (Amplitude Modulation to Amplitude Modulation) and AM-PM (Amplitude Modulation to Phase Modulation) (Ding, 2004). These effects should be considered also in this thesis and the method for overcoming these problems are investigated. The main impact of the memory effects is dynamic AM-AM and AM-PM which is discussed in this thesis. The technique that is introduced as the contribution of this thesis overcomes the problem of the memory effects. The other main problem while implementing the new predistortion technique is in calculating the inverse of the input signal which should be done by a divider. This function is not available in FPGAs and needs to be constructed by other blocks. This will be addressed in this thesis. The new method for complex division is introduced which has many advantages from the other dividers (Ercegovic, 2003; Agrawal, 2006). There are some other problems that are not very critical but need to be investigated specially the effects of gain factor on the convergence rate of the predistortion and also the effects of the hardware resources. Here the concentration is on these problems and study them. There are some