

# **UNIVERSITI PUTRA MALAYSIA**

# PROCESS CONSOLIDATION OF BORON STEAM AND EMITTER DIFFUSION IN PNP BIPOLAR TRANSISTOR FABRICATION

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Partial Fulfillment of the Requirements for the Degree of Master of Science

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## **DEDICATION**

To my children, Syazwani, Safiah and Sarah, You are my pride and inspiration.

*To my wife and life partner*, thank you for your continuous support, patience, encouragement and motivation.



Abstract of thesis submitted to the Senate of Universiti Putra Malaysia in partial fulfillment of the requirements for the degree of Master of Science

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#### Faculty: Engineering

Boron Steam is a process done after boron emitter diffusion for all PNP transistors and diodes. Boron emitter diffusion is a process to dope the emitter well with P-type dopant. The source of this dopant is in the form of liquid spun on the wafers and exposed to high temperatures. Boron steam is done to basically soften the residual liquid boron prior to cleaning for easy removal. This project will cover hardware comparison and recipe proposal that were used. The new consolidated process has resulted in comparable final in-line measurement of oxide thickness and test results. Reliability expectation was also met with 1000 cycles of Intermittent Operating Life test. Significant cost advantages were also achieved.



Abstrak untuk tesis ini dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi sebahagian dari keperluan untuk ijazah Master Sains

## PENGGABUNGAN PROSES PENGWAPAN BORON DAN RESAPAN PEMANCAR DIDALAM PEMBIKINAN TRANSISTOR DWIPOLAR JENIS PNP

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Pengwapan boron adalah salah satu dari proses yang dilakukan selepas proses resapan pemancar keatas semua transistor jenis PNP dan diod. Resapan pemancar dengan bendasing boron adalah proses di mana kawasan pemancar diperkayakan dengan bendasing jenis-P. Sumber bendasing jenis-P ini adalah dalam bentuk cecair yang disembur ke atas wafer untuk membentuk lapisan yang rata dan wafer itu kemudian didedahkan pada suhu yang tinggi. Pengwapan boron dilakukan untuk melembutkan lapisan baki boron yang berlebihan yang tidak digunakan. Ini adalah untuk memudahkan pembersihan lapisan baki di atas wafer. Projek ini akan meliputi perbandingan perkakasan yang digunakan dan cadangan resepi yang digabungkan. Proses baru yang telah digabungkan dapat memenuhi kesemua kehendak kritikal dalam pemprosesan dan juga ujian elektrik terakhir. Ujian keboleharapan yang dilakukan juga menunjukkan tiada sebarang masalah dengan proses baru. Terdapat juga penjimatan kos setelah melaksanakan projek ini.



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## LIST OF ABBREVIATIONS

P-type	majority carriers of charge are holes
N-type	majority carriers of charge are electrons
PNP	Transistor (emitter is P-type, base is N-type, collector is P-type)
NPN	Transistor (emitter is N-type, base is P-type, collector is N-type)
TEOS	Tetra Ethyl Ortho Silicate
PH <sub>3</sub>	Phosphine
SiO <sub>2</sub>	Silicon Dioxide
Si <sub>3</sub> N <sub>4</sub>	Silicon Nitride
PECVD	Plasma enhanced chemical vapour deposition
LPCVD .	Low Pressure chemical vapour deposition
LPCVD CpK	Low Pressure chemical vapour deposition Process capability index
СрК	Process capability index
CpK Å	Process capability index Angstrom (1 x 10 <sup>-10</sup> m)
ČpK Å САВ	Process capability index Angstrom (1 x 10 <sup>-10</sup> m) change action board
Å CAB IOL	Process capability index Angstrom (1 x 10 <sup>-10</sup> m) change action board Intermittent Operating Life
ČpK Å CAB IOL CMOS	Process capability index Angstrom (1 x 10 <sup>-10</sup> m) change action board Intermittent Operating Life Complimentary metal oxide semiconductor
ĈpK Å CAB IOL CMOS BiCMOS	Process capability index Angstrom (1 x 10 <sup>-10</sup> m) change action board Intermittent Operating Life Complimentary metal oxide semiconductor Bipolar complimentary metal oxide semiconductor



$B_2O_5$	Boron Pentoxide
B-75	Liquid boron in Toluene (Brand name)
UV	Ultra violet
DCE	Dichloro ethylene
HF	Hydrofluoric Acid
Al-Si	Aluminum Silicon
Hfe	transistor gain (direct current)
Vbef	Voltage drop between base and emitter
Vbcf	Voltage drop between base and collector
Vce	Voltage drop between collector and emitter
Icbo	Collector-base leakage
Icev	Collector-emitter leakage
BJT	Bipolar Junction Transistor

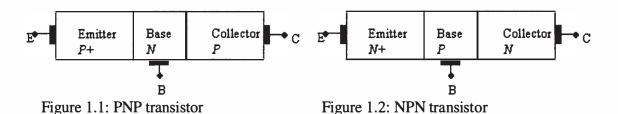


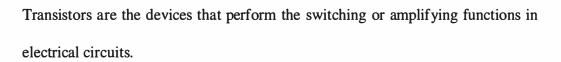
### **CHAPTER 1**

#### **INTRODUCTION**

This project is related to the fabrication of bipolar transistors and diodes. The bipolar transistor is a two-junction, three layer device in which the current can flow. One p-n junction can be modulated by interaction with another nearby p-n junction. The structure maybe either p-n-p or n-p-n, but only P-N-P devices will be discussed, since the N-P-N transistor does not go through the boron emitter diffusion nor the boron steam processing. However the results are applicable to N-P-N transistors with appropriate change of polarities. Figure 1.1 and 1.2 shows the PNP and the NPN bipolar transistor respectively. Bipolar transistors were the first type of solid state amplifying devices commercially available. The electrical characteristics of a bipolar transistor are determined primarily by the bulk properties of the semiconductor material used for its manufacture. The discrete devices and integrated circuits produced by the semiconductor industry up through the late 1960s were largely fabricated using bipolar technology. Due to their early technology lead and their intrinsic characteristics, bipolar devices continue to be used advantageously both as discrete components and as devices in integrated circuits. Today, bipolar integrated circuits and bipolar devices combined with CMOS devices in BiCMOS integrated circuits are significant factors in the marketplace.







The essential features of the bipolar transistors are:-

- Two junction diodes that share a common base region. This can form an n+pn or p+np bipolar transistor.
- > The emitter material is heavily doped compared to the base material.
- The lifetime of the minority carrier in the base is sufficient that these carriers can drift and diffuse to the base collector depletion region, where they are collected. The base width is the critical dimension in the transistor.
- The doping profiles in the base and collector must form a reverse biased diode with sufficient reverse breakdown voltage for the application.

### 1.1 Bipolar Integrated Circuit Process Flow

The fabrication processes for bipolar transistors, particularly as an element in an IC, are extremely varied. All processes, however, contain these basic elements:

- Formation of collector material
- Formation of the device isolation
- Formation of the base and emitter regions



An IC process for a traditional bipolar structure is shown in Figure 1.3

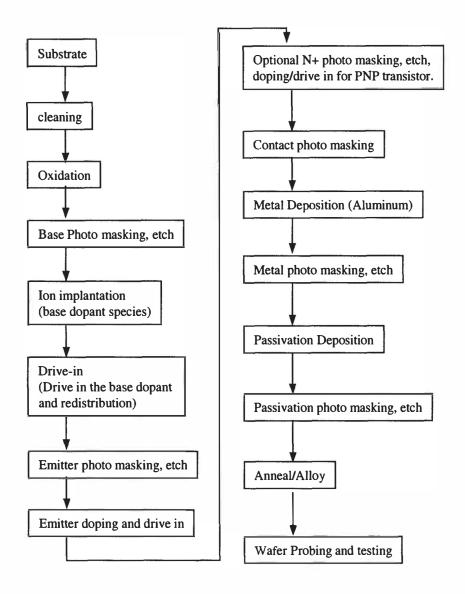


Figure 1.3. Simplified Bipolar Process Flow Chart[4].



The isolated regions formed within the n-epi tubs are used for the fabrication of the NPN bipolar transistors. The device cross section is shown in Figure 1.4, where the material marked by the small box is the active portion of the device.

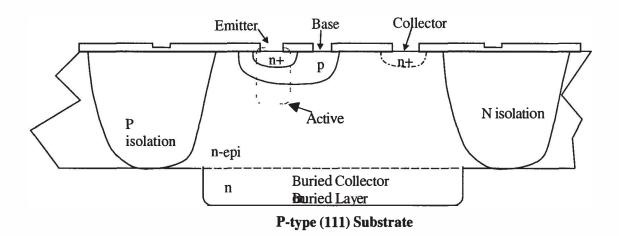


Figure 1.4: Bipolar device cross section [4]

## **1.2 Uses of Bipolar Transistors**

The primary uses of bipolar transistors and ICs are :-

As an amplifier (analog or linear). A small current is amplified to a much larger value by the transistor. Transistors used as amplifiers are usually operated in the small signal mode. In this mode, the changes in the currents flowing in the transistors are small compared to the bias currents. For linear applications, the individual process steps are modified to achieve higher device breakdown voltages and higher device current gains. This application typically requires thick epitaxial silicon layers and deep junctions.



As an electronic switch (logic or digital). A large current can be turned on or off by a small current. Transistors used as switches are operated in the large signal mode. In this mode, the transistor will typically be switched from cutoff to saturation. For digital applications, the individual process steps are modified to achieve the high packing density required for complex digital circuits. This application typically requires thin epitaxial silicon layers and shallow junction depth.

Both of these uses depend on the current amplification property of the bipolar transistor.

### **1.3 Statement of Problem**

PNP transistor fabrication cycle time is too long compared to the NPN transistor fabrication. On time delivery to customer is being affected by the PNP transistor fabrication due to additional steps in the process flow. Therefore, there is a need to find ways to reduce cycle time of the PNP transistor fabrication. Since boron steam consolidation to emitter diffusion has been identified as one of the potential and viable project, focus will only be to this consolidation project.



### 1.4 Objective of Project

The objective is to implement boron consolidation to emitter diffusion with minimum impact to manufacturing. Final electrical testing results have to be comparable. The new process should also meet reliability requirements.

### **1.5** Scope and Limitation

The scope of this project is limited to existing hardware that is already available. Due to this, there will be limitation to some of the experiments that can be carried out such as the steam temperature selection and post steam cleaning time.

## **1.6 Expected Outcome**

Since the wafer will not be subjected to any new material or processing, the outcome is expected to be positive. However due to the steam temperature increase, there could be some complications in final electrical response. This can be verified at final electrical testing.



### **CHAPTER 2**

### LITERATURE REVIEW

### 2.1 Introduction

Wafer fabrication is a very complex process whereby the entire process consists of many steps. In most cases these steps are repeated with different parameters. Proper sequencing and repetition of the oxidation, patterning and dopant addition operations can be used to introduce p- and n-type dopant atoms selectively into regions on a surface having dimensions ranging down to the submicron range. These steps are the basic elements of wafer fabrication [2]. In early process, before silicon, Germanium transistors were made by alloying the emitter and the collector regions to a thin slice of an appropriately doped semiconductor. This process did not allow good control of the emitter and collector geometries and resulted in base widths on the order of several microns. Consequently, in the beginning Silicon transistors were made by growing the emitter, base, and collector regions during the process of crystal growth from the melt. The next significant step was to develop a solid-state impurity diffusion process that allowed much tighter control over the device geometry and the base width. Alternatively, transistors could be produced by a double diffusion process in which p- and n-type diffusions were performed in succession from the same face of the wafer giving the impurity profiles needed [3].



A more commonly used process technology is the CMOS technology, whereby a totally different structure is fabricated, taking into consideration the requirement of today's needs. Low power consumption, low leakage requirements and low heat dissipation were among the motivations towards this change. Nevertheless the demands for bipolar is still increasing due to certain applications are performing better using this technology.

## 2.2 Bipolar Junction Transistor (BJT) Operations

The operation of an NPN transistor is explained in Figure 2.1, two brick type junction diodes share a central p-type material of initial width, W.

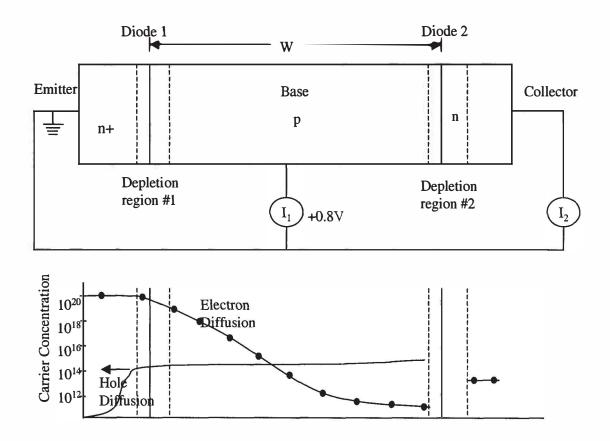


Figure 2.1. Two brick diodes forming a bipolar transistor [1].

