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FABRICATION AND CHARACTERIZATION OF O.5-um MOSFET BULK SILICON TECHNOLOGY ON THICK BONDED SILICON-ON-INSULATOR SUBSTRATE

WAN FAZLIDA HANIM ABDULLAH

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By

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March 2003

Chairman : **Dr. Roslina Mohd Sidek**

Faculty : **Engineering**

The effect of thick film Silicon-On-Insulator (SOI) substrate on device fabrication and performance is studied. Enhancement-type Partially-Depleted SOI MOS device is fabricated on bonded SOI (BSOI) substrate based on bulk silicon MIMOS 0.5 μm CMOS technology with full compatibility maintained. The substrate employed is commercially available with the specification 1.5 μm silicon device layer with ±0.5 μm within wafer variation on 2 μm buried oxide achieved by bonding followed by mechanical thinning. .

Prior to device fabrication, sacrificial oxidation is applied to adjust the top silicon layer thickness. Throughout the fabrication, monitoring steps using spectroscopic reflectometry technique are taken in ensuring enough silicon thickness is left on the top BSOI surface for device construction. To allow comparison of substrate effects, bulk silicon substrates are included in the fabrication as control wafers.

Three main electrical parameters were extracted from all sites of all the wafers. Bonded SOI (BSOI) substrate is observed to undesirably increase threshold voltage and decrease drive current capability. Sacrificial oxidation technique to adjust the silicon layer thickness worsens device performance and yield. However, BSOI substrate offers much improved off-state leakage current compared to bulk devices.

Further current-voltage sweep data analysis show that BSOI substrate improves the subthreshold slope, reduces the drain-induced barrier lowering effect and improves resistance towards latchup. Peculiar device characteristics typical to Partially-Depleted SOI devices were observed from the output characteristics. These include early breakdown voltage, negative conductance in the saturation region of body-contacted devices at high gate voltages and kink effect when the body is left floating.

The results show that SOI fabrication is achievable using existing bulk silicon fabrication technology. Even though devices on BSOI substrate show certain improvements in device characteristics, the full potential of the SOI structure could not be achieved with the thickness and uniformity of the BSOI substrate applied.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

FABRIKASI DAN PENCIRIAN PERANTI MOSFET 0.5-µm TEKNOLOGI SILIKON BONGKAH DI ATAS SUBSTRAT SILIKON-ATAS-PENEBAT TERIKAT

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Pengerusi : **Dr. Roslina Mohd Sidek**

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Kajian dilakukan ke atas kesan substrat silikon-atas-penebat (SOI) lapisan silikon tebal terhadap fabrikasi dan prestasi operasi peranti. Peranti MOS jenis peningkatan separa-susut difabrikasi atas substrat SOI terikat (BSOI) berdasarkan teknologi silikon bongkah 0.5-µm CMOS hak MIMOS dengan mengekalkan keserasian proses fabrikasi sepenuhnya. Substrat SOI yang digunakan boleh diperolehi secara komersil dengan spesifikasi lapisan silikon 1.5 µm dengan variasi ± 0.5 µm di atas oksida tertanam setebal 2 µm yang disediakan menggunakan teknik pengikatan diikuti dengan penipisan mekanikal.

Sebelum pemprosesan peranti bermula, pengoksidanan korban dilakukan bagi menipiskan lagi lapis silikon di atas penebat. Langkah pengawasan diambil sepanjang pemprosesan peranti bagi memastikan ketebalan yang mencukupi masih terdapat pada lapisan atas substrat untuk pembuatan peranti. Bagi membolehkan perbandingan kesan substrat dikaji, substrat silikon keseluruhan disertakan sepanjang fabrikasi sebagai wafer kawalan.

Tiga parameter elektrikal utama diekstrak dari setiap tapak peranti kesemua wafer. Substrat (BSOI) memberi kesan yang tidak dingini dengan meninggikan voltan ambang dan merendahkan daya arus. Teknik penipisan lapisan silikon secara pengoksidanan korban menerukkan lagi prestasi peranti dan peratusan penghasilan. Walau bagaimanapun, substrat BSOI menjadikan arus bocor status tutup jelas lebih baik berbanding peranti silikon keseluruhan.

Analisa lanjutan ke atas data arus-voltan menunjukkan substrat BSOI memperelokkan kecerunan bawah ambang, mengurangkan kesan perendahan kawasan susutan cetusan parit dan menambahkan kekebalan terhadap fenomena lekapan. Melalui pendemonstrasian ciri luaran arus-voltan, ciri peranti separa-susut SOI dapat diperhatikan. Antaranya adalah voltan runtuhan awal, konduksi negatif dalam kawasan tepu pada voltan get tinggi dan kesan penambahan mendadak pada arus parit apabila badan peranti dibiarkan terapung.

Hasil penyelidikan menunjukkan bahawa fabrikasi peranti SOI boleh dicapai menggunakan teknologi silikon bongkah. Walaupun peranti di atas substrat BSOI mempamirkan ciri peranti tertentu yang semakin baik, potensi struktur SOI tidak dapat dimanfaatkan sepenuhnya dengan ketebalan dan ketidak-seragaman substrat BSOI yang diguna-pakai.

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LIST OF ABBREVIATION

BESOI	Bond-and-Etch-Back Silicon-On-Insulator
BJT	Bipolar Junction Transistor
BSOI	Bonded Silicon-On-Insulator
CMOS	Complementary Metal-Oxide-Semiconductor
CV	Capacitance-Voltage
DIBL	Drain-Induced Barrier Lowering
FDSOI	Fully-Depleted SOI
g_D	Drain Conductance
g_m	Gate Transconductance
I_{DS}	Drain Current
I_{p+}	Current from PMOS source/diffusion region
IV	Current-Voltage
L_g	Gate length
LNPN	Lateral NPN bipolar transistor
MIMOS	Malaysian Institute of Microelectronics System
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NMOS	n-channel MOSFET
PDSOI	Partially-Depleted SOI
PMOS	p-channel MOSFET
r_D	Drain resistance
SIMOX	Separation by Implantation of Oxygen
SOI	Silicon-On-Insulator
VDS	Drain-to-Source Voltage
VFB	Flat-band Voltage
V_{p+}	Voltage at PMOS source/drain diffusion region
VPNP	Vertical PNP bipolar transistor
V_{PT}	Punchthrough Voltage
V_{SB}	Source-to-Substrate Voltage
V_T	Threshold Volatge
γ	Body Effect Parameter
λ	Channel-Length Modulation Parameter
σ	DIBL Parameter

CHAPTER 1
INTRODUCTION

1.1 CMOS Technology Development Summary

The core structure in the Complementary Metal-Oxide-Semiconductor (CMOS) technology is the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). This section provides a digest on the development of the MOSFET structure that promotes the progress of the CMOS technology making it the dominant logic technology in the electronics industry since the past three decades. The Silicon-On-Insulator (SOI) CMOS technology forms part of the picture in an effort to fuel the growth of CMOS technology.

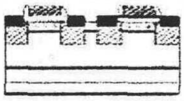
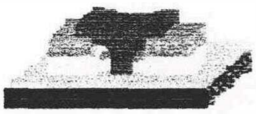
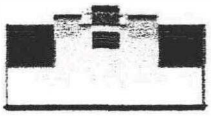
1.1.1 Evolution of the MOSFET

In pursuit of better performance and to satisfy the requirements of a wide variety of applications, the MOSFET goes through evolutionary changes involving scaling down of device dimensions and device architecture modification since its invention half a century ago. Guided by the scaling theory [1], downsizing CMOS achieves higher packing density, higher speed and lower power [2]. Exploring altered transistor structures and material modifications on the other hand seeks solutions to allow shorter channel length or to accomplish improved performance for a given channel length [3]. In relation to successfully accomplishing improved packing density, Moore's Law predicted the number of components per chip would double every one to two years that was proven in the technology trend for the next 25 years [4]. The smallest transistor built in 1965 had a channel length of 25 μm [5]. In 1999, it was predicted that between 2003 and 2006, transistors with a minimum channel length of 0.05 μm would be fabricated with the accompanying lower power-supply of 1.2 V and lower threshold voltage near 0.25 V [6]. Confirming the prediction in 2001, 50 nm gate length transistors for embedded processor core applications was reported [7].

The CMOS industry issues 15-year forecasts of technology roadmaps to project future trends and to identify potential roadblocks in order to focus on the needs and develop timely solutions [8]. The most recent published projection to date, the 2001 International Technology Roadmap for Semiconductors [9], presents the technology trend projection up to year 2016 with a targeted physical gate length of 9 nm and 11 nm for high performance logic and low operating logic power requirements respectively. Some of the important challenges highlighted by the 2001 ITRS are in the front-end process referring to the fabrication of the MOSFET transistors [10]. Among the expected barriers include important physical phenomena such as gate-to-channel, body-to-drain and source-to-drain tunnelling currents [11]-[12], severe short channel effects [13]-[14] and problems associated with wiring [15].

Among the proposed solutions to achieve the 2001 ITRS projection [16] require device architecture modifications in order to allow further scaling at room temperature without reduction in performance improvement rate [17]. The most recent of the state-of-the-art research efforts include exploring gate insulator material with higher dielectric constant [18] and non-classical device structures such as ultra-thin body Silicon-On-Insulator (SOI), band-engineered transistors incorporating SiGe or strained silicon channel and double-gate/surround-gate devices as shown in Table 1.1.

Table 1.1: Non-classical CMOS demonstrating device architectural modification aiming towards higher performance, higher transistor density and lower power dissipation. [19]

Device	Schematic Cross-Section	Concept	Advantages
ULTRA-THIN BODY SOI		Fully Depleted SOI	-Improved subthreshold slope - Vt controllability
BAND-ENGINEERED TRANSISOTR		SiGe or Strained si Channel: bulk or SOI	- Higher drive current - Bulk and SOI compatible
VERTICAL TRANSISTOR		Double-gate or surround-gate structure	-Higher drive current -Lithography Independent Lg
FINFET			-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND
DOUBLE-GATE TRANSISTOR			-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND

1.1.2 SOI CMOS Technology

The Silicon-On-Insulator MOSFET structure is one of many device architectural modifications that have caught the attention of the CMOS industry since the late 1970s. The initial motivation towards the implementation of the structure is based on its radiation hard properties, orienting the application of SOI devices towards space and military purposes [20]. From the 80s onwards, the trend of SOI research is directed towards low-voltage, low-power and high-speed properties and applications [21].

SOI technology leads to steeper subthreshold slope, absence of CMOS latchup, smaller off–state leakage current and reduced parasitic capacitances [22] leading to improved speed-power products. Added advantage with SOI design is the versatility of SOI structure design owing to additional physical parameters available for manipulation towards optimized scaling [23]. Furthermore, SOI enables increased chip functionality without the cost of major process equipment changes involving higher resolution lithography tools. Contemporary SOI applications encompass CMOS VLSI circuits, bipolar, power, Broadband LANs, micro-displays and MEMS circuits [24].

Cost factor involved in SOI substrate fabrication is an obstruction for the migration from bulk silicon to SOI technology. However, recent developments have shown that several semiconductor companies have begun to produce SOI devices commercially in moderate volumes to benefit from the potential gains [25]. Further device design making full use of the SOI substrate raises the possibility of reducing process steps thus compensating the cost increase.

1.2 Research Objectives

Despite the fiscal implication being a barrier to the implementation of SOI research, the interest of local microelectronics industry to venture the possibilities of SOI technology would be inevitable. For this research effort, the research work is implemented in MIMOS Berhad that runs the first wafer fabrication facility in Malaysia. This is the first fabrication attempt involving SOI substrates on the MIMOS production line. As SOI technology research work has yet to be reported in Malaysia, the strategy adopted would be to implement an existing bulk silicon technology to SOI substrates whilst maintaining its compatibility, only allowing