UNIVERSITI PUTRA MALAYSIA

LOW POWER STANDARD CELL LIBRARY DESIGN FOR APPLICATION SPECIFIC INTEGRATED CIRCUIT

ASRAL BIN BAHARI JAMBEK

LOW POWER STANDARD CELL LIBRARY DESIGN FOR APPLICATION SPECIFIC INTEGRATED CIRCUIT

By

ASRAL BIN BAHARI JAMBEK

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of Requirement for the Degree of Master of Science

August 2002

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Master of Science

LOW POWER STANDARD CELL LIBRARY DESIGN FOR APPLICATION SPECIFIC INTEGRATED CIRCUIT

By

ASRAL BIN BAHARI JAMBEK

August 2002

Chairman : Dr. Roslina Mohd. Sidek
Faculty : Engineering

With the expansion of portable and wireless electronics product in the current market demand, the focus of designing VLSI system has shifted from high speed to low power domain. This requires chip designers to minimize power consumption at all design level such as system, algorithm, architecture, circuit and technology.

The objective of this work is to develop low power CMOS standard cell library to be used in application specific integrated circuit (ASIC) design flow. The design methodology focuses on all aspect of circuit design: transistor size, logic style, layout style, cell topology, and circuit design for minimum power consumption. The standard cell library is targeted for general-purpose application, especially in microprocessor design. For rapid design implementation, the library is designed to be used together with the commercial logic synthesis and automatic cell placement and routing tools. Results show that the microprocessor targeted to the low power library gives 44% power saving compared to the conventional library, with both designs operate at the same clock frequency of 50MHz.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

REKEBENTUK KOLEKSI SEL PIAWAI BERKUASA RENDAH UNTUK LITAR BERSEPADU BERAPLIKASI SPESIFIK

Oleh

ASRAL BIN BAHARI JAMBEK

Ogos 2002

Pengerusi : Dr. Roslina Mohd Sidek
Fakulti : Kejuruteraan

Dengan perkembangan peralatan elektronik mudah alih dan tanpa wayar dalam permintaan pasaran semasa, fokus merekabentuk sistem VLSI telah beralih daripada berkelajuan tinggi kepada berkuasa rendah. Keadaan ini mengkehendaki perakabentuk cip meminimumkan penggunaan kuasa pada semua peringkat, contohnya peringkat sistem, algoritma, seni bina, litar dan teknologi.

Objektif penyelidikan ini adalah untuk merakabentuk koleksi sel piawai berkuasa rendah bagi membina litar bersepadu beraplikasi spesifik (ASIC). Penyelidikan ini menfokuskan pada setiap aspek rekabentuk litar elektronik seperti mensaizkan transistor, tatacara logik, gambaran litar dan topologi litar bagi mengurangkan penggunaan kuasa. Koleksi sel piawai berkuasa rendah ini direkacipta khas untuk aplikasi-pelbagai, terutamanya di dalam membina pemprosessan mikro. Untuk mempercepatkan tugas ini, sel ini direka khas bagi digunakan bersama-sama dengan peralatan sintesis logik dan pendawaian automatik. Hasil penyelidikan ini menunjukan bahawa pemprosesan mikro yang menggunakan koleksi sel ini mampu

mengurangkan penggunaan kuasa sebanyak 44% berbanding dengan sel konvensional, dengan kedua-duanya beroperasi pada frekuensi pemasaan yang sama, iaitu 50MHz.

ACKNOWLEDGEMENTS

I would like first to thank our God Almighty for the countless blessing throughout our lives, and for giving us a drop from His sea of knowledge, which enable us to reach at this stage.

It gives me a great pleasure to express my immense gratitude towards my guide Dr. Roslina Mohd. Sidek, Department of Electrical and Electronics, Universiti Putra Malaysia, for her most competent guidance and encouragement during my research work. Her unparalleled enthusiasm has made this project a success.

I am indebted to Dr. Bambang Sunaryo Suparjo and Dr. Mohd. Rais Ahmad, En. Rahman Wagiran and En. Nasri Sulaiman for their valuable discussion and help. They also encourage me time and again.

Last but not least, my special thanks go to my parents for their understanding and support, and to my wife, who could keep me in a good mood during the last period of this work.

This thesis submitted to the Senate of Universiti Putra Malaysia has been accepted as fulfillment of the requirement of Master of Science. The members of the Supervisory Committee are as follows:

ROSLINA MOHD. SIDEK, Ph.D.
Faculty of Engineering,
Universiti Putra Malaysia.
(Chairperson)

RAHMAN WAGIRAN, MSc.
Faculty of Engineering,
Universiti Putra Malaysia.
(Member)

NASRI SULAIMAN, MSc.
Faculty of Engineering,
Universiti Putra Malaysia.
(Member)

AINI IDERIS, Ph.D,
Professor / Dean,
School of Graduate Studies,
Universiti Putra Malaysia

Date:

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
BSIM	Berkeley Short-Channel IGFET Model
CAD	Computer Aided Design
C_{area}	Area Capacitance
C_{bottom}	Bottom Plate Diffusion Capacitance
C_{diff}	Diffusion Capacitance
C_{eff}	Effective Capacitance
C_{gate}	Gate Capacitance
C_{gb}	Gate-Bulk Capacitance
C_{gd}	Gate-Drain Capacitance
C_{gd0}	Gate-Drain Overlap Capacitance
C_{gs}	Gate-Source Capacitance
C_{gs0}	Gate-Source Overlap Capacitance
C_{int}	Interconnect Capacitance
C_{j0}	Junction Capacitance
C_{jsw}	Side-wall Junction Capacitance
C_L	Load Capacitance
CMOS	Complementary Metal-Oxide-Semiconductior
C_{ox}	Oxide Capacitance
CPL	Complementary Pass Logic
C_{sw}	Side-wall Capacitance
f_{clk}	Clock Frequency
Gnd	Power Supply (Ground)
HDL	Hardware Description Language
IC	Integrated Circuit
$I_{leakage}$	Leakage Current
I_{sc}	Short-Circuit Current
PDP	Power Delay Product
$P_{leakage}$	Leakage Power
$P_{short-circuit}$	Short Circuit Power

$P_{switching}$	Switching Power
SNM	Static Noise Margin
SPICE	Simulation Program with Integrated Circuit Emphasis
SPL	Single Pass Logic
t_{clk}	Clock Period
t_{ho}	Hold Time
t_{ox}	Oxide Thickness
t_p	Average Propagation Delay
t_{pd}	Propagation Delay (Fall)
t_{pu}	Propagation Delay (Rise)
t_{su}	Setup Time
TTL	Transistor-Transistor Logic
VDD	Power Supply
V_{dsat}	Saturation Voltage
V_{IH}	Maximum Input Voltage
V_{IL}	Minimum Input Voltage
Vin	Input Voltage
VLSI	Very Large Scale Integrated Circuit
V_{NH}	Noise Margin (High)
V_{NL}	Noise Margin (Low)
V_{OH}	Output Voltage (High)
V_{OL}	Output Voltage (Low)
V_{out}	Output Voltage
V_{Tn}	N-type transistor threshold Voltage
V_{Tp}	P-type transistor threshold Voltage

CHAPTER 1

INTRODUCTION

Today, we are in the era of expending multimedia demand. Our information-oriented society depends heavily on a network infrastructure base on personal mobile computing and communication devices. These devices are the basis for the handheld personal computer, portable laptops, cellular phones, digital cameras, video games, and pagers [1,2,3]. To be effective, the processor in such a device must consume very low power.

Historically, VSLI designers have focused on circuit speed as the performance criteria. Large gain in terms of performance and silicon area has been made for various integrated circuit designs such as microprocessors, digital signal processing (DSP) and memory. In general, small area and high performance are two conflicting constraints. The IC designers' activities have been involved in trading off these constraints. The power dissipation issue was not a design criterion, but as a secondary requirement [4].

With the recent development, power dissipation has becoming an important design constraint. Several reasons underlie the emerging of low power design:

- Battery-operated devices are suffered from low battery lifetime. Although the battery industry has been making efforts to develop batteries with higher energy capacity, the progress rate is quite slow [5]. The expected improvement of the energy density is only 40% for the next 5 years. With the increase of chip performance double every year, the battery technology has come to its limit.

- With the increase of integration density and operation speed, more power are dissipated as heat resulting in the increase of chip temperature. The cost associated with the packaging, cooling and fans required by these systems to remove the heat is increasing significantly.

- Another issue related to high power dissipation is reliability. With the generation of on-chip high temperature, failure could arise due to interconnect fatigue, package related failure, electrical parameter shift and elctromigration.

Technology improvements in the last few decades have succeeded in reducing power consumption [6, 7]. Trends such as using CMOS instead of bipolar devices and reduction in feature size of lithographic processes have served to reduced power dissipation, although other objectives, namely high integration and speed, were the primary goals of such improvement.

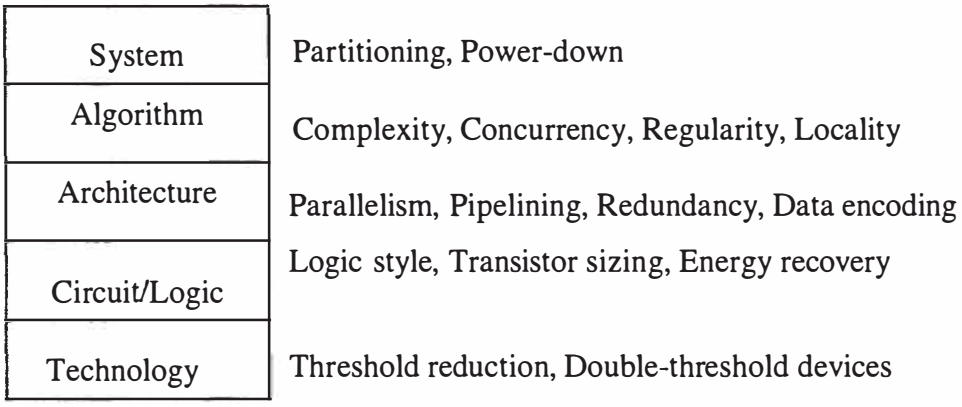

Figure 1.1: A design hierarchy for low power methodology

In practice, VLSI designers are bounded to the available technology. Thus, most of the effort to reduce the power is highly dependent on the design approach, which mainly to reduce the source of power dissipation wherever possible. Many researches have been done in this area, which span at different level of design abstraction. Figures 1.1 shows different design hierarchy using top-down approach in which optimizations are possible.

At system and algorithm level, the power can be reduced as early as possible during the design stage. Since it has a great influence to the final design specification, a highest gain in power saving can be achieved at this level.

For some application, large amounts of power are wasted while the system is in idle. The power consumption can be reduced significantly by using a power management scheme to shut down idle components. Result has shown that the system with power management was measured to be less than 50% of that without power management [8].

At architectural level, parallelism and pipelining can be exploited to improve the performance of low-voltage circuits [9]. This method allows the system to perform computation at the same throughput as obtained by using the conventional architecture at a lower supply voltage. The disadvantage of this method is an increase in chip area due to additional registers needed.

The next level in the hierarchy of low power techniques resides at the logic and circuit layer. Several important choices such as logic block composition and mapping will impact overall power consumption. The decision of logic block optimisation has been studied in great detail in [10]. In this paper, a power reduction of 20% is reported by reorganising the complex block. Techniques such as energy recovery circuit [11], dual-threshold circuits [12] and operating digital logic at sub-threshold region [13] are the promising approach to achieve ultra-low power requirement.

Once the system and architecture of a design is decided, it is left to the circuit designer to realised the final design at the transistor level. The success in designing the low power system is now heavily dependent on the approach for manipulating the transistor to perform the required logic function. As far as standard cell library is concerned, optimisation for power can be done at circuit and logic level. Many parasitic parameters that cause large amount of power dissipation could be controlled at circuit level. Therefore, developing a low power cell libraries is crucial, thus providing effective solution to low power design.

1.1 Research Objective

The objective of the work is to design a low power standard cell library for the use in application specific integrated circuit (ASIC) design. The standard cell library consists of various types of logic gates ranging from a simple inverter to asynchronous register circuit. Each circuit are designed and characterized for the use in designing bigger module, i.e. microprocessor. All designs are done in 0.5µm CMOS technology, and they are targeted for the use together with logic synthesis and automatic place and route tools.

1.2 Research Approach

In this work, the relevant component which impact power as well as delay in ASIC design will be identified. As mentioned, power as a figure of merit should be considered concurrently with delay; a power reduction with proportional delay increase achieved no net advantage. In this phase, the CMOS power dissipation properties and the existing power reduction technique for CMOS digital circuit will be focused.

It is the interest of this research to identify which circuit techniques should be applied to minimized power consumption if one also wishes to reduce delay. Those approaches, which show the most promise, are the subject of our most intense focus. This will be done in the second phase of this work, where analysis and comparison

will be made on the possible technique by investigating ideas for power reduction in digital logic circuit.

The circuit will be designed based on standard cell methodology, which is important in industry today. These cells were extensively characterized for power and delay under wide range of input slope and output load. The standard cell library is targeted for designing ASIC, especially for microprocessor design.

The actual design implementation was performed automatically using logic synthesis tools. Once the circuit blocks have been assembled, the contribution of physical effect will be estimated using a placement and routing tools, which determine the wiring characteristic based on actual interconnect length.

Given the logic and physical description of the design, timing analysis was performed using static delay information from the characterised standard cells. Power was determined using logic simulator which counted switching events from the signal activity. The property of the microprocessor will be analysed and compared in order to study its effectiveness with respect to overall performance.

1.3 Thesis Organization

This thesis is organised into five chapters. There are introduction, literature review, methodology, result and discussion and the last is conclusion and future work.

The first chapter is the introduction. It gives a brief introduction about the whole work and the objective of every section in it.

Second chapter gives the fundamental and essential background for the CMOS technology and circuit issue. The sources of power dissipation are discussed in detail and the possible minimising technique are also included.

Chapter 3 highlights the methodology and the step taken to accomplished this project. It discussed the method followed to develop the low power library and how it is implemented into microprocessor design.

Chapter 4 discussed the result obtained from the simulation and significant finding during the development of the library. It shows the way the results were dealt with and how it is used to minimise the power in the cell library. The performance of the microprocessor targeted using the library is analysed and the overall improvement in term of power and speed are measured.

Finally, chapter five summarised the conclusion drawn from the project presented in the thesis. Further work and area of improvement are also proposed for better result and quality in the future.

The library was tested and found to be working satisfactorily and the goal has been achieved. However, improvement still can be made to this work as discussed in chapter 5.

The Appendices contain the useful information, and will be cross-referenced throughout the thesis to assist for better understanding.