UNIVERSITI PUTRA MALAYSIA

DESIGN OF DIRECT SEQUENCE CODE DIVISION MULTIPLE ACCESS (DS-CDMA) WIRELESS TRANSMITTER USING FIELD PROGRAMMABLE GATE ARRAY (FPGA)

KHALID ELTAHIR MOHAMED OSMAN

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By

KHALID ELTAHIR MOHAMED OSMAN

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, In Fulfilment of the Requirement for the Degree of Master of Science

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Dedicated

To you…
…Dear mother…. for making out of us the
person who can present such a work...for doing all this with pleasure……

To you…
…. Dear brother Amin…. the person who lead to
success life…and taught me how to face my struggles…..

To you…
… Dear brothers, sisters, nephews and niece…
Mohamed, Awad, Nura, Fathia, Sadia, Asma, Omima, Ahmed, Sumia, Mahmoud,
Amna, Mohamed, lina, Dania…

To all the glory inside you…

To you…
…love…thanks…and my simple effort…

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

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Chairman: Professor Borhanuddin Mohd. Ali. Ph.D.

Faculty: Engineering

This thesis describes the DS-CDMA wireless transmitter design using FPGA (Field Programmable Gate Array), which has been adopted in many wireless access technologies. Four separate blocks have been designed using digital approach to form the transmitter circuit diagram using the oscillator, the PN-code generator, the Parity Check, and the BPSK modulator. The Synopsys software has been used for the design synthesis and simulation; the VHDL (Very High Speed Integrated Circuit Hardware Description Language (VHDL)) program was used for coding and FPGA for compiling and downloading the simulation in FPGA cards.

The DS-CDMA wireless transmitter was designed to transmit with data rates up to 2 Mbps. The transmitted signals were carried out with a 40 MHz carrier frequency.

VHDL files were created for each element of the wireless transmitter. Each file was simulated and synthesized using FPGA compiler II. The control block was added for timing purposes and for framing the coded data. One bit parity was added to the data frame containing 16 serial bits.

The top-level design file was initiated using VHDL for the combined elements of the DS-CDMA wireless transmitter including the control block. The results of simulated and synthesized top-level design file using FPGA compiler II were downloaded into the Xilinx XSV300 FPGA board.

This study has demonstrated the design of DS-CDMA wireless transmitter with higher data rates using FPGA. It has also improved the performance and quality of the transmitted data by including error detection and correction.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

REKA BENTUK PENGHANTAR WAYARLES CAPAIAN KOD BERBILANG DIVISI-JUJUKAN TERUS (DS-CDMA) DENGAN MENGGUNAKAN SUSUN TERTIB GET LAPANGAN BOLEH PROGRAM (FPGA)

Oleh

KHALID ELTAHIR MOHAMED OSMAN

Ogos 2002

Pengerusi : Profesor Borhanuddin Mohd. Ali, Ph.D.

Fakulti : Kejuruteraan

Projek ini menghuraikan reka bentuk penghantar wayarles capaian kod berbilang divisi –jujukan terus (*DS-CDMA)* menggunakan susun tertib get lapangan boleh program (*FPGA)* yang telah digunakan dalam banyak teknologi capaian wayarles. Empat blok berasingan telah direka bentuk dengan pendekatan digit, menggunakan oksilator, penjana kod-PN, semakan pariti dan pemodulat BPSK untuk membentuk gambar rajah litar penghantar. Implementasi dan perisian sintesis digunakan untuk menggabungkan keseluruhan komponen. Perisian Sinopsis digunakan untuk reka bentuk dan simulasi. Program *VHDL (Very High Speed Integrated Circuit Hardware Description Language)* digunakan untuk pengkodan, dan *FPGA (Field Programmable Gate Array)* digunakan untuk kompilasi dan muat turun simulasi ke dalam kad *FPGA*.

Penghantar wayarles *DS-CDMA* direka bentuk untuk melakukan penghantaran dengan kadar data sehingga 2Mbps. Isyarat yang dihantar dilaksanakan oleh pembawa berfrekuensi 40 MHz.

Fail *VHDL* dicipta untuk setiap unsur pada penghantar wayarles. Setiap fail disimulasi dan disintesis dengan menggunakan Pengompil II *FPGA*. Blok kawalan ditambahkan bagi maksud pemasaan dan kerangkaan bagi data terkod. Satu bit pariti ditambahkan pada kerangka data yang mengandungi 16 bit sesiri.

Fail reka bentuk paras tertinggi diwujudkan dengan menggunakan *VDHL* untuk unsur-unsur (penghantar wayarles *DS-CDMA*) yang digabungkan dan termasuk blok kawalan. Hasil reka bentuk paras terrtinggi tersimulat dan tersintesis yang menggunakan pengompil II *FPGA* telah dimuat turunkan ke dalam papan *FPGA* Xilina XSV300.

Kajian ini telah menunjukkan reka bentuk penghantar wayarles *DS-CDMA* dengan kadar data lebih tinggi menggunakan *FPGA*. Kajian ini juga telah memperbaiki prestasi dan kualiti data yang dihantar dengan cara memasukkan pengesanan dan pembetulan ralat . Kaedah yang disyorkan yang berasaskan pemodelan perilaku memberi keupayaan simulasi yang unggul.

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TABLE OF CONTENTS

Page

LIST OF TABLES

Table **Page**

LIST OF FIGURES

Figure **Page**

LIST OF ABBREVIATIONS

AMPS	Advanced Mobile Phone Service
CDMA	Code Division Multiple Access
DS	Direct Sequence
FH	Frequency Hopping
FHMA	Frequency Hopping Multiple Access
FHSS	Frequency Hopping Spread Spectrum
FSK	Frequency Shift Keying
JTIDS	Join Tactical Information Distribution System
LAN	Local Area Network
LPI	Low Probability of Intercept
NMT	Nordic Mobile Telephone
PN	Pseudo-Noise
RF	Radio Frequency
SNR	Signal to Noise Ratio
SS	Spread Spectrum
SSMA	Spread Spectrum Multiple Access
TACS	Total Access Communications System
TxPC	Transmit Power Control
UPM	Universiti Putra Malaysia

CHAPTER 1

INTRODUCTION

1.1 Background of the Study

Code Division Multiple Access (CDMA) is a radically new concept in wireless communications. It has taken cellular radio systems by storm with its potential to dramatically increase both the system capacity and service quality. CDMA is a *spread spectrum* technology in that it spreads the information from a narrowband signal over a much broader bandwidth.

One of the most important concepts to cellular telephony is *multiple access* which allows several users to be supported simultaneously. In other words, several users share a pool of channels with any user able to use any channel and no channel assigned to any user. A channel is therefore merely a part of the radio resource, temporarily allocated for a call. *Multiple access* is therefore just how a radio spectrum is divided into channels and how the channels are allocated to the several users of the system.

CDMA architecture is based on the spread-spectrum technique (Tabbane, 2000), initially developed by the military because of its usefulness in tactical environments. It is used, for instance, in GPS as part of the tactical information distribution system (JTIDS). The core principle of spread spectrum is to use noise-like carrier waves in, as the name implies, a bandwidth much wider than that required for simple point-to-point communication at the same data rate. Militarily there were two advantages – it is impossible to jam by the enemy (anti-jam, or AJ) and masks the fact that communication is taking place. Thus, in military parlance, it was called *low probability intercept* (LPI). Although first used in the early days of World War II, it was only in 1978 that spread-spectrum techniques were proposed for high capacity cellular mobile communications systems.

There are two main techniques involved - Frequency Hopping (FH) and Direct Sequence (DS). DS is also called Code Division Multiple Access (CDMA). In both techniques, synchronization of the transmitter and receiver is required. Both use a pseudo-random carrier, but the carrier is created in different ways.

Rahman (2000) recorded that the Direct Sequence Spread Spectrum (DS-SS) uses a code sequence with a bit rate higher than the digital data bit rate to be transmitted. The carrier signal is modulated by the code sequence resulting in a wideband signal from the transmitter. The process is reversed at the receiver to regenerate the data transmitted.

In CDMA, each station is allocated a random sequence or code. This sequence is unique to the station and must be orthogonal or quasi-orthogonal (i.e. decorrelated)

with all the other sequences. In FH-CDMA, the code is used to generate a unique hopping sequence. In DS-CDMA, the code is used to make a quasi-random (i.e. similar to noise) high rate transmitted signal combined with the information spread the spectrum.

A transmitter is linked to the receiver by radio waves to the allocated base station, or cable line (wired) to a computer allowing the computer to transmit/receive data from a similarly equipped remote control.

1.2 Problem Statement

There are many types of electronic circuits used for transmission with different options for DS-CDMA. The use of some circuitry was dictated by the availability of a particular IC, or because a portion of a quad gate was yet unused. Some circuits using passive components also need high power to drive the circuit. The addition to the high power needed the passive circuits is altered to decrease the circuit operations of transmission, when the transmitter operates with long time duration. These effects appear as thermal heat that increases the passive components values and decrease the efficiency of transmission. However, the circuit used is easy to implement and simplify.

For these reasons, DS-CDMA wireless transmitter using FPGA is regarded as a promising technique for future CDMA networks. The transmitter is mainly used digital components such as flip-flops, gates, etc., which leads the transmission in higher performance.

1.3 Significance of the Study

Wireless communications with mobile and cellular radio technology is experiencing its fastest growth ever, particularly in the past 10 years. It has already progressed from the first generation (1G) to second generation (2G) which uses Frequency Division Multiple Access (FDMA) and Time Division Multiple Access (TDMA). In the new millennium the world is about to receive the third generation, which is predicated on higher data rate and better spectrum efficiency to enable wireless data communication in full multimedia.

In 3G, the information transferred is not limited to having voices, images and digital data separately. Users will have full coverage and mobility for 144 kbps (preferably 348 kbps) and eventually up to 2 Mbps limit. With this wideband, users are able to access the information in full multimedia form, wirelessly and with better quality.

1.4 Objectives of the Thesis

The objectives of this study were to:

1. Study the spread-spectrum DS-CDMA concept, especially the PN coding system.
2. Study BPSK modulation in the DS-CDMA system.
3. Implement PN coding and BPSK modulation in the DS-CDMA transmitter circuit using digital transmission.
4. Design, simulate and synthesize the PN coding, BPSK modulation, Oscillator and Parity Check, using the VHDL source code.

5. Create the top-level design file for the DS-CDMA wireless transmitter using the VHDL source code for PN coding, BPSK modulation, Oscillator and Parity Check, using the FPGA compiler II.
6. Download the design into a Xilinx FPGA board.

1.5 Constraints of the Project

This thesis describes the DS-CDMA wireless transmitter design using FPGA. The DS-CDMA wireless transmitter is expected to transmit at data rates up to 2 Mbps with error detection and 40 MHz carrier frequency. The Synopsys package was used as the simulation and synthesis tool (FPGA compiler II and VHDL). The Synopsys package allows easy reconfiguration of the transmitter. The design steps using this software depend mainly on the design components and the system configuration. The applicability of certain frequencies depends on the system application and design scenario. For this transmitter, the frequency carrier depends on the hardware (FPGA board) and the system components of the transmitter circuit. The FPGA board has a maximum frequency of 100 MHz. Some frequency dividers had to be used as shown in Appendix 22 to slow the frequency down to below this speed. For this project, a clock of 2 MHz was used. For the simplified design, a 40 MHz speed was used with two frequency dividers, multiplying the clock speed by 2 and 10 times.

The function of any communication system is to carry information – as voice, video or digital signals. To carry the information, a band is required. To send more information, a broader band or more time is required with a trade-off between the two. Other factors are also involved – the power pushing the signal through and the

clutter (noise) in the band. Shannon's law of channel capacity relates the maximum rate of data transfer as follows:

$$Capacity = bandwidth * log_2\left(1+\frac{signalpower}{noisepower}\right)$$

with capacity in bits per second, bandwidth in hertz and signal and noise powers in the same physical units, such as watts. From the equation, the relationship between capacity and bandwidth is linear. Doubling the bandwidth therefore doubles the capacity. In contrast, the effects of signal power and noise power are logarithmic and therefore less dramatic. A large increase in power will result in a less than proportionate increase in the capacity (Schweber, 1991).

The XSV board has a variety of interfaces for communicating with the outside world: parallel and serial ports, Xchecker cable, a USB port, PS/2 mouse and keyboard port and 10/100 Ethernet PHY layer interface. There are also two independent expansion ports, each with 38 general-purpose I/O pins connected directly to the Virtex FPGA. The board can be configured through the parallel port, serial port, Xchecker cable or from a bit stream stored in the 16 M bit Flash RAM. The Flash RAM can also store data for use by the FPGA after the configuration is complete. The complete features of the XSV FPGA board were discussed in Appendix 23.

To extend the project to the analog portion of the transmitter, a special version of VHDL called VHDL-AMS can be used for analog-mixed signal and might be able to be used for analog system design. However, VHDL-AMS capability has to be investigated first as a feasibility study.