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Uninterruptible Power Supply Topology Based on Single-Phase Matrix Converter with Active Power Filter Functionality

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Abstract: This study introduces a novel uninterruptible power supply (UPS) configuration that integrates active power filter (APF) capabilities within a single-phase matrix converter (SPMC) framework. Power disruptions, particularly affecting critical loads, can lead to substantial economic damages. Historically, conventional UPS systems utilized dual separate converters to function as a rectifier and an inverter, without incorporating any power factor correction (PFC) mechanisms. Such configurations suffered from diminished power density, compromised reliability, and spatial limitations. To address these issues, this research proposes an enhanced UPS design that incorporates APF features into the SPMC. The focus of this investigation is on the efficiency of alternating current (AC) to direct current (DC) conversion and the reverse process utilizing this advanced UPS model. The SPMC is selected to supplant the rectifier and inverter units traditionally employed in UPS architectures. A novel integrated switching strategy is formulated to facilitate the operation of the UPS in either rectifier (charging) or inverter (discharging) modes, contingent upon the operational state. The performance and efficacy of the devised circuit design and switching technique are substantiated through simulations conducted in MATLAB/Simulink 2019 and empirical evaluations using a test rig. The findings demonstrate that the voltage generated is sinusoidal and synchronized with the supply current, thereby minimizing the total harmonic distortion (THD) and enhancing both the power factor and the transition efficiency of the UPS system between its charging and discharging states.

Keywords: single-phase matrix converter; uninterruptible power supply; pulse width modulation; rectifier; inverter

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1. Introduction

The reliability and quality of electricity supply are crucial determinants of sustainable energy delivery. In recent times, the adoption of uninterruptible power supply (UPS) systems has surged, largely propelled by advancements in the global manufacturing landscape [1,2]. Within this domain, the demand for a dependable and high-quality power source is paramount, particularly for operations deemed critical and susceptible to disruptions [3–6].

A traditional UPS framework is characterized by three principal elements: a rectifier, an inverter, and a static bypass switch, depicted in Figure 1. The static bypass switch is designed to seamlessly transition the power source for critical loads to an auxiliary supply, effectively segregating it from the primary source until reintegration with the grid is achieved. The rectification process is facilitated by a bridge diode configuration, devoid of any sophisticated control mechanisms [7,8]. However, such conventional UPS configurations are beleaguered by challenges, including substantial physical bulkiness due to the amalgamation of three distinct components, elevated levels of total harmonic distortion (THD), and diminished power factor efficiency [9].

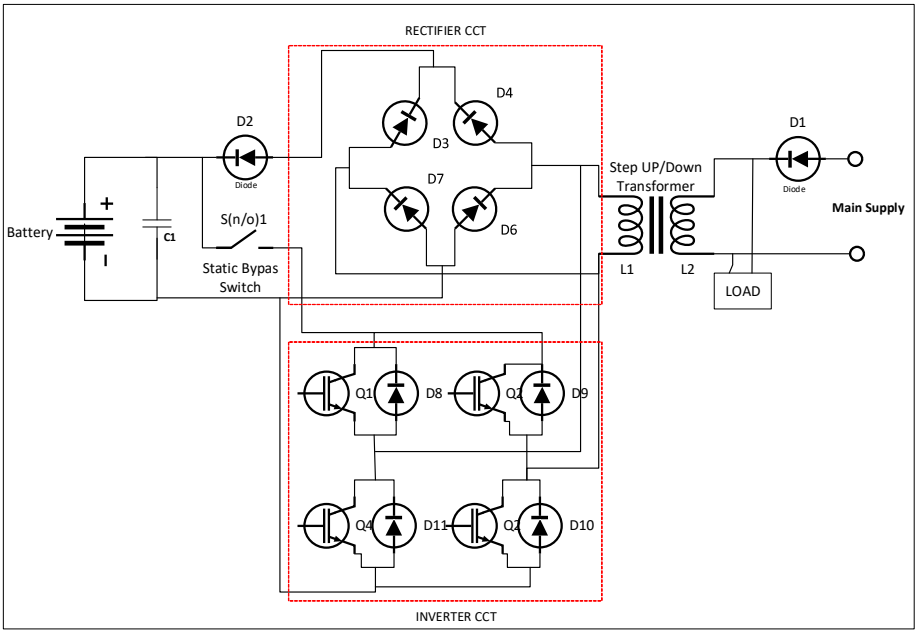


Figure 1. Typical UPS system.

The matrix converter (MC) has garnered significant interest for its efficacy in AC–AC conversion processes [10–12], with its conceptual foundations laid by Gyugyi in 1976 [13]. It operates across all four quadrants of switching technology, presenting a viable alternative to the conventional voltage source inverter approach [14,15]. Following its inception, the single-phase matrix converter (SPMC) was conceptualized by Zuckerberger [16], necessitating four bidirectional switches for its assembly as illustrated in Figure 2. These switches are adept at facilitating bidirectional current flow while also being capable of voltage blockade in both directions [11,17], utilizing insulated gate bipolar transistors (IGBT) switches renowned for their appropriateness in medium-frequency switching and high-current applications suitable for medium power scenarios.

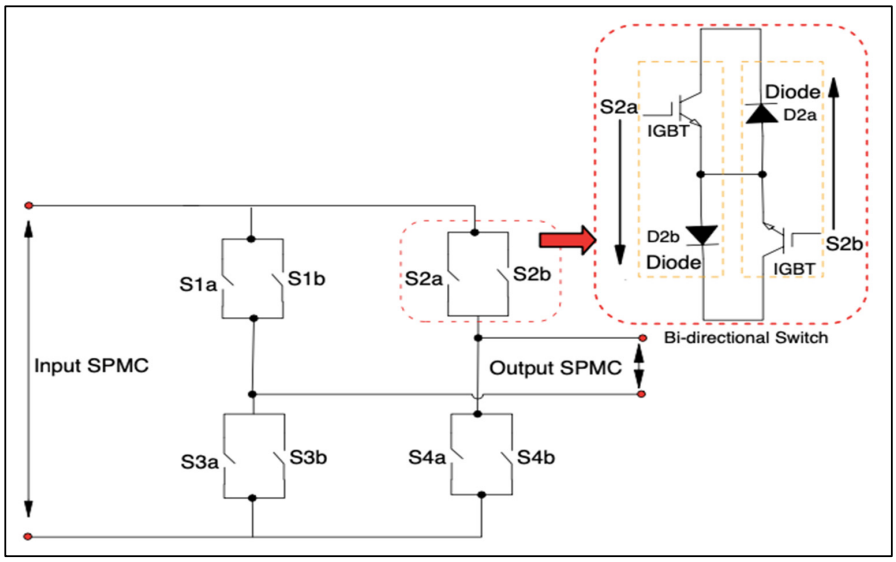


Figure 2. SPMC topology and its bidirectional switch.

Recent scholarly endeavours have explored various topologies to enhance rectifier and inverter functionalities. Among these, the SPMC stands out as a singular solution for both controlled rectification and inversion processes, as explored in this study. The discourse extends to control algorithms for both processes within the SPMC framework, incorporating

secure commutation techniques to mitigate voltage and current surges potentially harmful to switching apparatus [18–20].

The foundational premise of utilizing SPMCs for UPS applications was posited in 2006 [21], introducing novel switching integration algorithms for rectification and inversion functions. Subsequent enhancements to these algorithms aimed at optimizing UPS operations were documented [22]. Nonetheless, these investigations did not adequately address power quality, contributing to considerable harmonic disturbances.

Advancements in employing SPMCs as a UPS system have evolved to include active power filter (APF) capabilities, initially introduced in [2]. This initiative was modelled and simulated via MATLAB/Simulink, employing secure commutation strategies within the switching algorithms while integrating APF features. Additionally, pioneering research on wireless power transfer (WPT) from UPS to load demonstrated more than 90% efficiency in power transfer, though it remained confined to simulation stages [23].

Notwithstanding these developments, the absence of empirical verification in laboratory settings has left the efficacy of the switching strategies unconfirmed. An initial evaluation of these strategies, as outlined in [24], reveals significant opportunities for refinement in the UPS system's switching mechanisms.

Consequently, this paper articulates the development of an innovative switching integration algorithm, enhancing an UPS circuit topology that amalgamates rectifier and inverter functions within a singular framework predicated on SPMCs. This novel approach, incorporating APF capabilities, aims at rectifying distorted supply currents. This study marks the inaugural laboratory validation of the proposed system, offering an exhaustive assessment of its harmonics mitigation efficacy.

2. Bidirectional Switch Power Losses

The SPMCs are controlled utilizing a combination of power semiconductor devices, namely insulated gate bipolar transistors (IGBTs) and diodes, which operate as switching elements alternating between the conduction, blocking, and switching states in cyclical fashion. In each of these states, a power dissipation component is generated, resulting in heating of the semiconductor devices and contributing to the total power losses. The power dissipation of the devices is contingent upon the operating conditions of the converter (output frequency, switching frequency, modulation strategy, voltage and current operating levels, load characteristics, etc.). An analytical modeling approach for semiconductor losses in matrix converters is described and presented in [25]. The conduction and switching losses are modeled through simple mathematical expressions based on the ideal behavior of the device. The total average power losses over a fundamental period for any device has been formulated in [26] as:

$$P_{avg} = \frac{1}{T}\int_0^T p(t)dt \tag{1}$$

where

$p(t)$ is devices instantaneous dissipated power.
T is fundamental output current period.

The power dissipation of a semiconductor device at an arbitrary time instant t is equivalent to the mean conduction and switching losses incurred within the device over the switching period $t + T_{sw}$ subsequent to t [27], as illustrated in Figure 3. This methodology facilitates the derivation of simplified continuous time power loss expressions by approximating the instantaneous power losses as:

$$P(t) \cong P_{cond}\,(t) + P_{sw}\,(t) = P_{cond}\,(t) + P_{on}\,(t) + P_{off}\,(t) \tag{2}$$

where $P_{cond}\,(t)$ and $P_{sw}(t)$ are the average conduction losses and average switching losses at each switching period, respectively. In this research, the UPS circuit schematic using SPMC topology is depicted in Figure 4. The power losses for IGBTs and diodes are enough to consider just one IGBT (for example S1a) and one diode (for example D1b) to calculate

SPMCs' power losses. In general operation of SPMCs for the positive cycle, the current flows through S1a and D1b and S4a and D4b, and for negative cycle, S2a and D2b and S3a and D3b. The total average power losses of IGBTs (S1a) can be expressed as follows:

$$P_{S1a}(t) \cong P_{cond/S1a}\,(t) + P_{sw/S1a}\,(t) = P_{cond/S1a}\,(t) + P_{on/S1a}\,(t) + P_{off/S1a}\,(t) \quad (3)$$

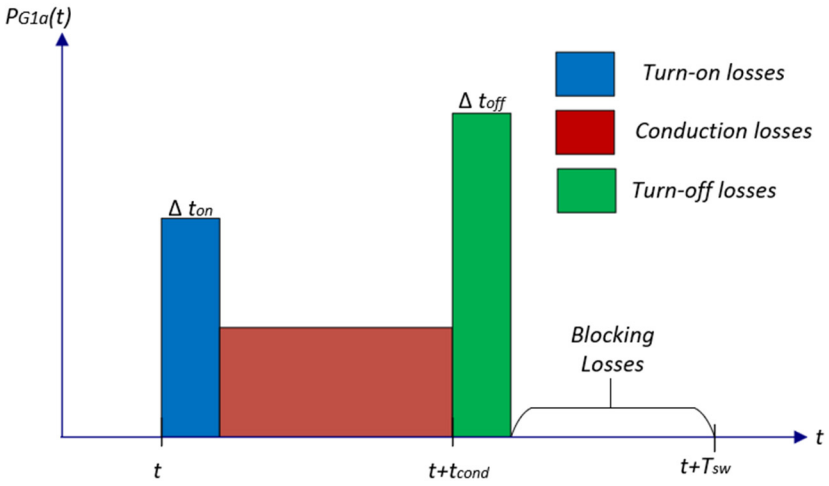


Figure 3. Schematic instantaneous IGBT power losses in a T_{sw} interval.

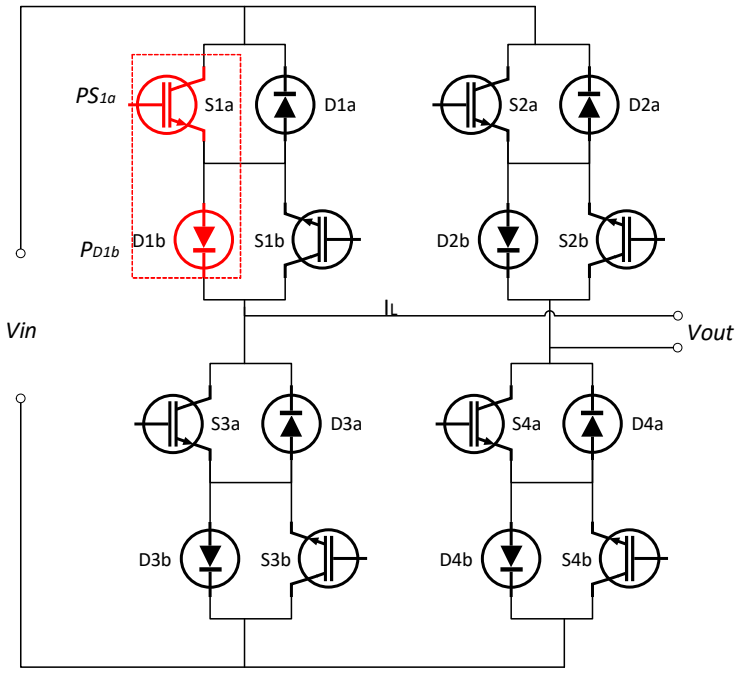


Figure 4. SPMC topology circuit bidirectional switch (IGBTs and diodes).

The detail expression explanation has been described in [28] and Appendix D. Thus, the average power losses of the IGBT $P_{S1a}(t)$ can be calculated as below:

$$P_{S1a}(t) = V_{S1a}(t)I_{S1a}(t)D_{S1a}(t) + \frac{E_{on/S1a}(t)}{T_{sw}} + \frac{E_{off/S1a}(t)}{T_{sw}} \quad (4)$$

$$P_{S1a}(t) = \left(V_{\frac{t}{S}} + a_S I_{S1a}^{b_S}\right)\left(I_M \sin(\omega_o t)\right)\left(\tfrac{1}{2}[1 + M\sin(\omega_o t + \varphi_o)]\right) + \left(\frac{hI_{S1a}^{k}(t)}{T_{sw}}\right) + \left(\frac{mI_{S1a}^{n}(t)}{T_{sw}}\right) \quad (5)$$

In the analysis of diode circuits, only two primary forms of power loss merit consideration: conduction losses and turn-off losses. The turn-on and blocking losses have been omitted from this analysis due to their negligible contribution to the total power dissipation described in [28,29] and Appendix D. A detail of the D_{1b} schematic instantaneous dissipated power can be appreciated in Figure 5. Thus, the $P_{D1b}(t)$ can be described as below:

$$P_{D1b}(t) \cong P_{cond/D1b}\,(t) + P_{sw/D1b}\,(t) = P_{cond/D1b}\,(t) + P_{off/D1b}\,(t) \tag{6}$$

$$P_{\frac{cond}{D1b}}(t) = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} V_{D1b}(t) I_{D1b}(t) dt = \frac{1}{T_{sw}} \int_{t}^{t+t_{cond/D1b}+\Delta t_{off}} V_{D1b}(t) I_{D1b}(t) dt \\ = V_{D1b}(t) I_{D1b}(t) D_D(t) dt \tag{7}$$

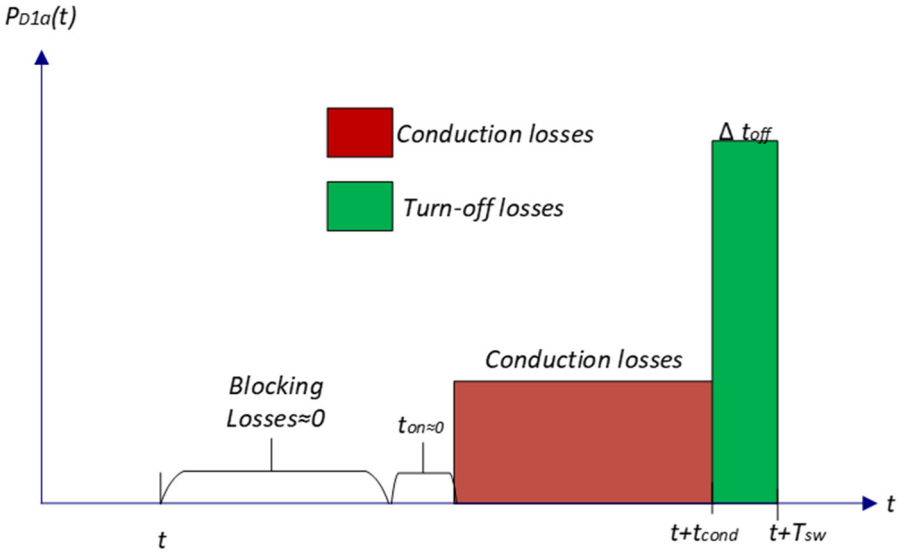


Figure 5. Schematic instantaneous of diode power losses in T_{sw} interval.

Total power losses diode (D1b) can be expressed as below:

$$P_{D1b}(t) \approx\ V_{D1b}(t) I_{D1b}(t) D_D(t) + \frac{E_{off/D1b}(t)}{T_{sw}} \tag{8}$$

As derived in details in Appendix D, then

$$P_{D1b}(t) = \left(V_{t/D} + a_D I_{D1b}^{b_D}\right)(I_M \sin(\omega_o t))\left(\frac{1}{2}[1 - M\sin(\omega_o t + \varphi_o)]\right) + \left(\frac{0.5 I_{rr}\ 0.5 V_{dc} t_b}{T_{sw}}\right) \tag{9}$$

In this work, turn-on and turn-off energy losses has been calculated under certain test conditions as well as the modelling parameters of the IGBT and diode switching losses can be found in [27] and parameter on the data sheet for IGBT BUP314D and Diode IN4118. The parameters are depicted in Table 1, and the total losses for typical dan proposed UPS are depicted in Table 2 based on expressions (5) and (9).

In the context of the impact on the number of diodes and switches employed in the UPS system, Table 2 presents a comparative analysis of the devices and switches utilized in a typical UPS system and the proposed UPS system. The conventional UPS system necessitates 13 diodes and switch, comprising 8 diodes, 4 IGBTs, and a bypass switch to facilitate rectifier and inverter operations. Conversely, the proposed UPS system incorporates 4 bi-directional switches, encompassing 8 diodes and 8 IGBTs, which enable the system to execute both rectifier and inverter operations, while the proposed system has 18.75% more devices and switches than the conventional system. The total power losses for the proposed UPS are 455.6W, while those for the typical UPS are 289.8W. However, it

retains the salient benefits of a compact system size, high power quality, low harmonic, and unity power factor. The proposed UPS notably, the paramount feature of the proposed novel advancement in single-phase UPS system design is the utilization of a singular circuit topology to perform both rectifier and inverter operations. Both operations can be controlled accordingly which cannot be done by the typical UPS system, in which the rectifier is based on uncontrolled operation. This attribute contributes to the realization of a high-power density power converter system, aligning with the power electronics technological roadmap, which aims to increase power density, efficiency dan reliability, and robustness.

Table 1. Parameter for IGBT and diode power losses.

State	IGBT Parameters	Diode Parameter
On-state	$V_{t/S} = 0.875$, $a_S = 0.028$, $b_s = 0.745$	$V_{t/D} = 0.8$, $a_D = 0.005$, $b_D = 1$
Turn-on	$h = 1.21 \times 10^{-3}$ mJ, $k = 1.65$,	-
Turn-off	$m = 0.027 \times 10^{-3}$ mJ, $n = 1.183$	*peak* I_{rr}= 25, $t_b = 0.030$ s
Applied voltage	$V_{dc} = 12$ V	
Fundamental frequency	$f_{out} = 50$ Hz	
Switching frequency	$f_{sw} = 5$ KHz	
Modulation	$M = 0.75$	
Peak current	$I_M = 1$ A	
Power factor	$\varphi = 0.74$rad	

Table 2. Number of switches used in UPS.

Device	Total Losses/Device	Proposed UPS	Typical UPS
		Number of Devices (Losses)	Number of Devices (Losses)
IGBT	41.45 W	8 (331.6 W)	4 (165.8 W)
DIODE	15.50 W	8 (124 W)	8 (124 W)
Total Losses	56.95 W	455.6 W	289.8 W

3. Topology of UPS System

The envisioned UPS architecture, utilizing the SPMC topology, is illustrated in Figure 6. This diagram, as previously noted, showcases a system solely comprising a single converter based on the SPMC topology, capable of functioning both as a controlled rectifier and a controlled inverter. The SPMC is strategically designed to switch roles between a rectifier (under standard conditions) and an inverter (during power disruptions), thereby obviating the necessity for distinct rectifier and inverter circuits found in conventional UPS designs. Figure 7 provides an intricate view of the circuit layout for the proposed rectifier and inverter configuration, notably absent of any filtering mechanisms. To facilitate its role in the UPS, a voltage sensor apparatus is employed to monitor the supply waveform within the circuit. This sensor plays a pivotal role in managing the transition between charging (rectifier mode) and discharging (inverter mode) operations within the UPS system.

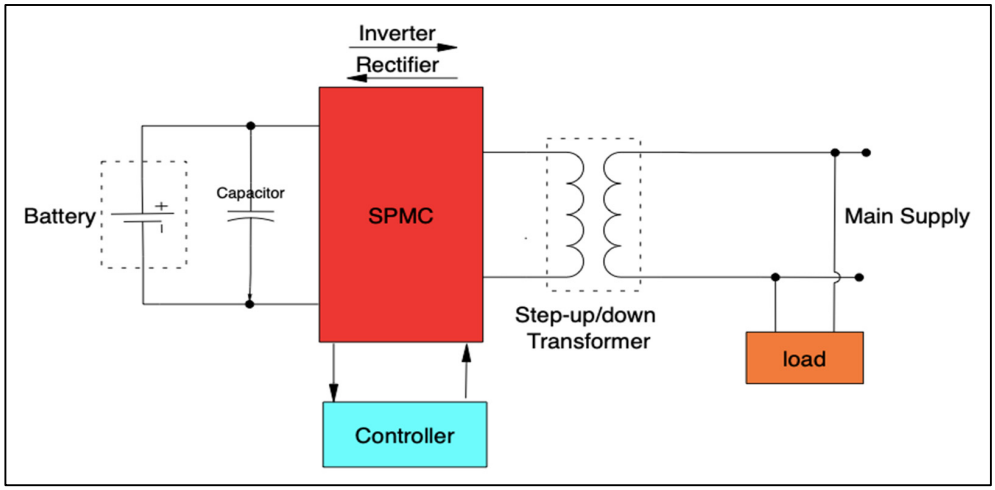


Figure 6. The proposed UPS system.

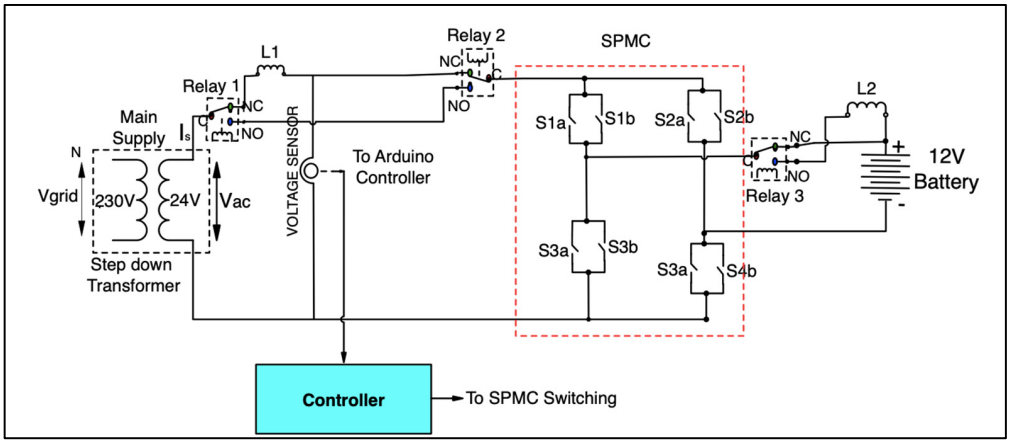


Figure 7. The proposed UPS circuit without filter.

4. Topology of UPS System with APF Functionality

The enhancement of the UPS framework is achieved through the integration of SPMC topology alongside APF capabilities. The APF feature is specifically designed to mitigate harmonic distortions arising from non-linear load activities. In this research, the elimination of harmonic constituents from the non-sinusoidal supply current is facilitated through an innovatively designed APF, which leverages a current control loop (CCL) strategy employing a boost technique. This APF function effectively compensates the supply current, rendering it sinusoidal and synchronized with the supply voltage waveform, as depicted in Figures 8a and 8b, respectively. To ensure system stability and enhance performance, the switching frequency for the controlled rectifier equipped with APF functionality was predetermined at 10 kHz, complemented by proportional and integral (PI) gains.

Figure 9 presents an intricate schematic of the circuit design for the rectifier function, enhanced with APF capabilities. To fulfill the requirements of the APF, an additional component, an inductor labeled L1, is incorporated to serve as the boost inductor. Furthermore, a current sensing device is deployed to monitor the supply current within the CCL framework. The CCL itself is composed of several key components: an absolute circuit, a subtraction circuit, a PI controller, and a comparator. This arrangement facilitates the generation of a sinusoidal reference signal, closely aligned with the supply waveform.

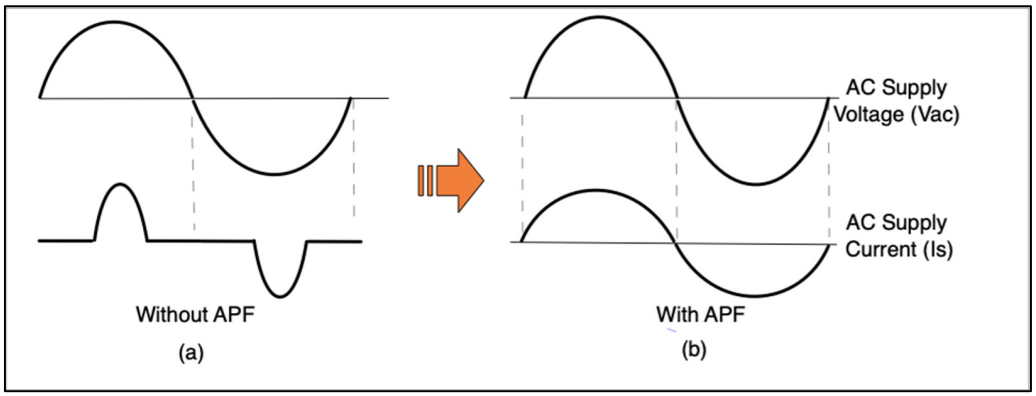


Figure 8. Comparison waveforms of rectifier connected to RC load (**a**) without APF and (**b**) with APF.

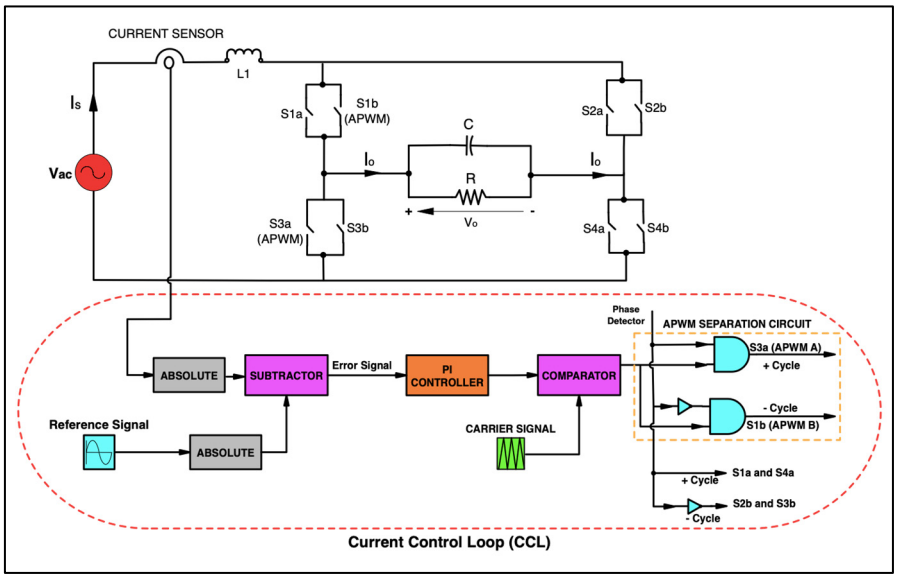


Figure 9. Rectifier with CCL.

4.1. APF Mathematical Treatment Modeling

The mathematical treatment of the boost inductor is formulated based on Figure 10. The circuit operation can be divided into two stages. Stage 1 represents the circuit operation during the pair of switches S1a and S3a are turned 'ON'. During this time, the current from the supply voltage flows through S1a and S3a and is defined as I_{13}. Stage 2 represents the circuit operation during the pair of switches S1a and S4a are turned 'ON'. At this time, the current from the AC supply flows through the pair of switches S1a and S4a and is defined as I_{14}.

The inductor current is linearly ramped from I_{13} to I_{14} at stage 1, as shown in Figure 11. During this period, the boost inductor charges energy. The equation for this interval (defined directly as S_{13}) with relationship between voltage supply V_{ac} and inductor voltage V_L can be stated as:

$$V_{ac} = V_L \tag{10}$$

$$V_{ac} = L\left[\frac{I_{14-I_{13}}}{S_{13}}\right] \text{ or } L\frac{\Delta I}{S_{13}} \tag{11}$$

Thus,

$$S_{13} = \frac{\Delta IL}{V_{ac}} \tag{12}$$

Figure 12 shows the simplified circuit for the stage 2. During the pair of S1a and S4a are turned 'ON' (S_{14}), and the energy from L1 is transferred to the load voltage V_o.

Therefore, the current of L1 decreases linearly during I_{14}, and thus the supply current I_S in this interval can be written as:

$$I_s = I_{L1} = I_{14} \quad (13)$$

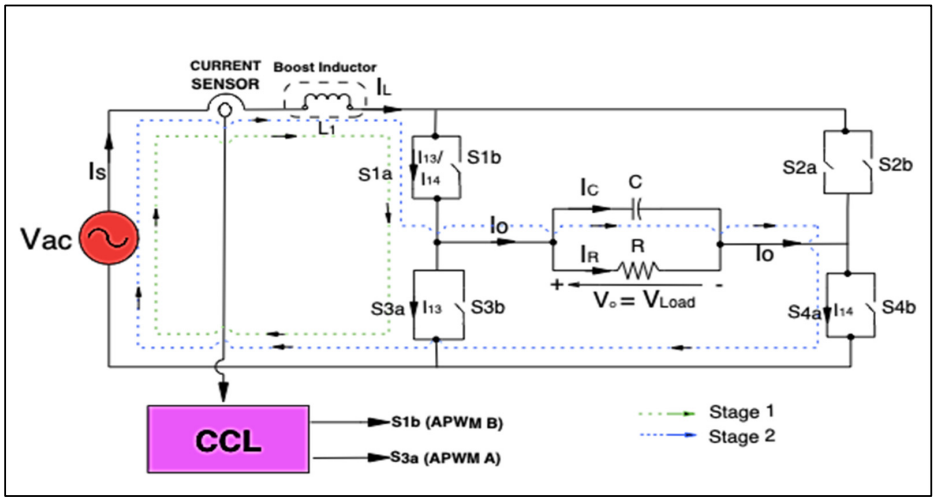


Figure 10. Boost inductor with SPMC circuit.

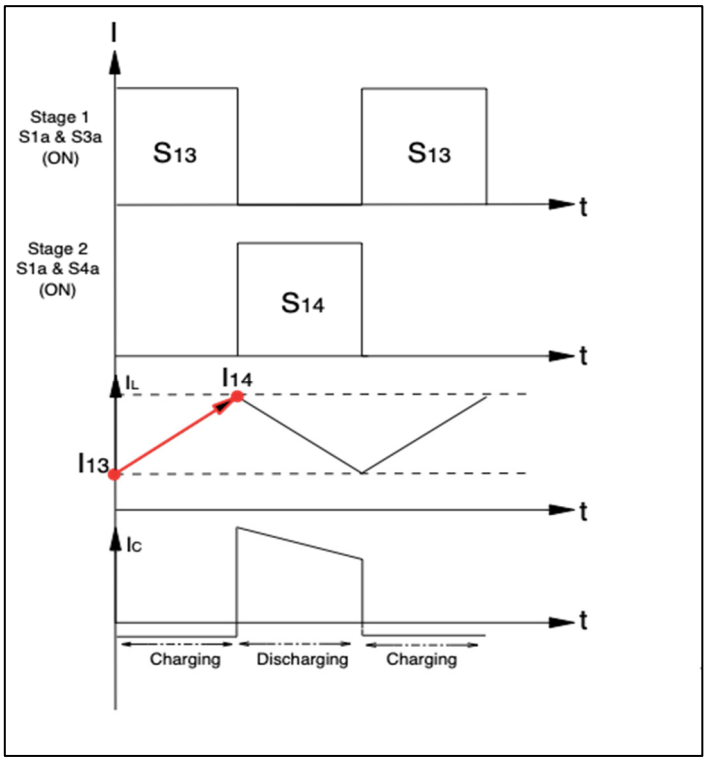


Figure 11. Waveforms for mathematical treatment of boost inductor.

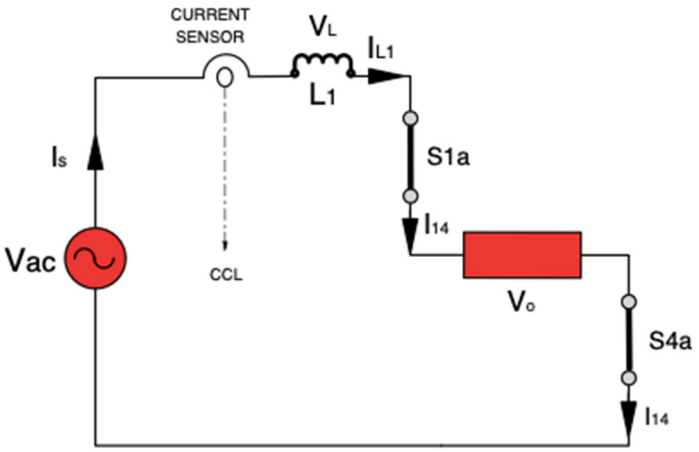


Figure 12. Circuit for mathematical treatment of boost inductor.

Meanwhile, voltage supply V_{ac} is

$$\begin{aligned} V_{ac} &= V_L + V_o \\ V_{ac} &= L\left[\frac{I_{13-I_{14}}}{S_{14}}\right] + V_o \end{aligned} \tag{14}$$

or can be written as for stage 2:

$$\begin{aligned} V_{ac} &= -\left(L\frac{\Delta I}{S_{14}}\right) + V_o \\ S_{14} &= \frac{\Delta I.L}{V_o - V_{ac}} \end{aligned} \tag{15}$$

From Equations (13) and (14), both can be written as

$$\Delta I = \frac{V_{ac}S_{13}}{L} = \frac{(V_o - V_{ac})S_{14}}{L} \tag{16}$$

From Equation (16), the boost inductor can be determined by

$$L = \frac{V_{ac}S_{13}}{\Delta I} \tag{17}$$

Meanwhile, the slope of the ripple current waveform m, as shown Figure 13, is given by

$$m = \frac{2A}{T/2} = \frac{4A}{T} = 4Af_s \tag{18}$$

where A is the maximum permitted peak of ripple current and f_s is the switching frequency. Otherwise, m also can be written as

$$m = \frac{\Delta I}{S_{13}} \tag{19}$$

In this work, the maximum peak to peak ripple is 1% from the line current, which is 1.7 A. By rearranging Equations (18) and (19),

$$L = \frac{V_{ac}S_{13}}{\Delta I} = \frac{V_{ac}}{4Af_s} \tag{20}$$

Using the circuit parameters A is 0.085 A, f_s is 10 kHz and V_{ac} is 12 V_{rms}, the value of L can be determined as

$$L = \frac{12}{4 \times 0.085 \times 10k} = 4mH$$

If the average capacitor current i_c is same as the load current i_o and the capacitor supplies the energy to the load during S1a and S3a (S_{13}) are turned ON, the peak-to-peak ripple voltage capacitor ΔV_c can be calculated as

$$\begin{aligned} \Delta V_c &= V_c - V_c(S_{13}) \\ &= \frac{1}{c}\int_0^{S13} i_c dt = \frac{1}{c}\int_0^{S13} i_o dt \end{aligned} \tag{21}$$

The value of output voltage ripple for the load will be considerable during the line inductor energizing period and load capacitor discharging period. The output voltage ripple is given

$$\frac{dV_{load}}{V_{load}} = \frac{\delta T}{RC} \tag{22}$$

where R is the load resistance, C is the capacitance, and δ is duty cycle ratio.

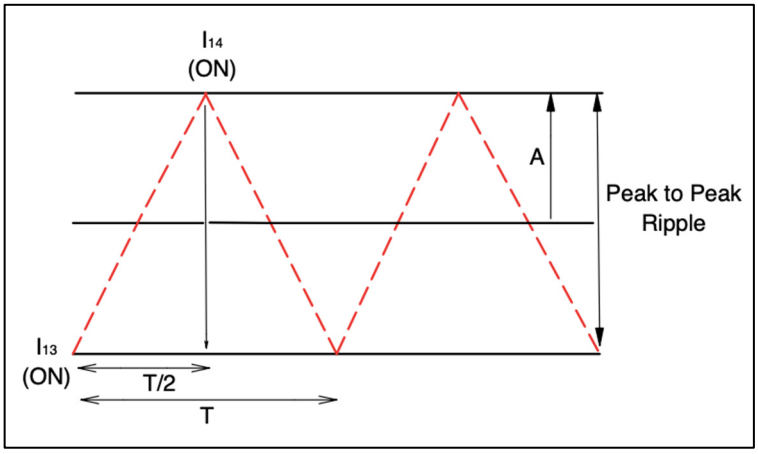


Figure 13. Peak-to-peak ripple current.

The mathematical treatment of APF is driven by the CCL to control the charging and discharging modes of operation of the boost inductor, as shown in Figure 14.

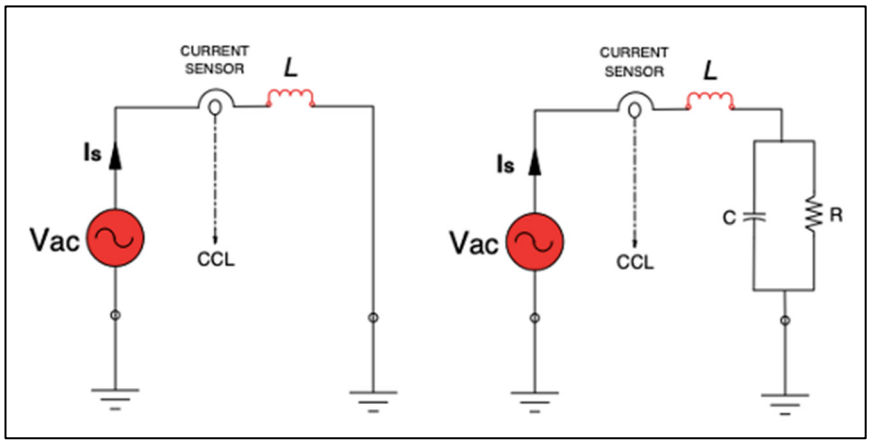


Figure 14. Circuit of APF configuration by (**a**) charging inductor and (**b**) discharging inductor.

The V_{ac} can be represented as:

$$V_{ac}(t) = V_{ac}\sin(\omega t) \tag{23}$$

where ω is the angular frequency of the fundamental component. The summation of supply current I_s with distortion components by using RC load can be written as

$$I_s(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \theta_n) \tag{24}$$

where I_n is amplitude of harmonic order n, and θ_n is its phase. For implementation of APF in the system, I_s can be written as

$$I_s(t) = I_1 \sin(\omega t + \theta_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n) \tag{25}$$

The second part is the non-sinusoidal component and should be removed accordingly. The CCL is the crucial part of the rectifier operation to eliminate the non-sinusoidal component and to ensure that the supply current later becomes sinusoidal and in phase with V_{ac}. To simplify the discussion of CCL, the circuit operation can be divided into nine stages, as shown in Figure 15.

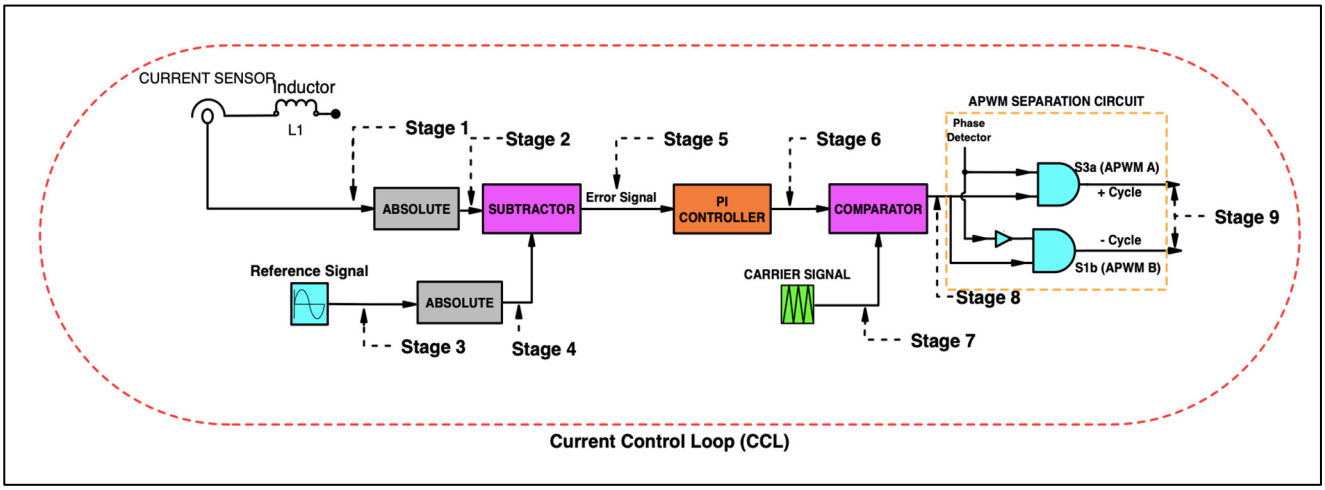


Figure 15. Stage configuration of CCL.

At the initial phase, the current sensor detects the supply current I_S, providing a crucial input to the CCL. This sensor is adept at identifying the waveform distortions in the supply current as previously discussed.

During the second phase, the bipolar distorted supply current waveform undergoes transformation into a unipolar waveform, courtesy of the absolute circuit. This conversion facilitates a forthcoming comparison with a unipolar carrier signal. The construction of the absolute circuit involves the utilization of two precision operational amplifiers (op-amps) and five precision resistors, as illustrated in Figure 16. In scenarios where the input signal exhibits a positive cycle, the output from op-amp $A1_{a1}$ turns negative, causing diode $D1_{a1}$ to exhibit reverse bias. Conversely, diode $D2_{a1}$ enters a state of forward bias, effectively completing the feedback circuit around op-amp $A1_{a1}$ via resistor $R2_{a1}$ and establishing an inverting amplifier configuration. The op-amp $A2_{a1}$ then aggregates the output from op-amp $A1_{a1}$, applying a gain factor of -2, alongside the input signal which is subject to a gain factor of -1, resulting in an overall gain of +1. When the input signal is in its negative cycle, diode $D1_{a1}$ assumes a forward bias, enabling the feedback loop around op-amp $A1_{a1}$, while diode $D2_{a1}$, being reverse-biased, remains non-conductive. Consequently, op-amp $A2_{a1}$ inverts the input signal, yielding a positive output voltage that encapsulates the absolute magnitude of the supply current, irrespective of whether it is in its positive or negative state.

Let us consider the case with $R2_{a1} = R3_{a1} = R$ and $R1_{a1} = R4_{a1} = R5_{a1} = 2R$. The circuit operation is divided into two intervals. During interval 1 (positive half-cycle), V_{ac} is positive, and $V1_{amp1} = -V_{ac}$. The voltage at the output $V0_{a1}$ of op-amp $A2_{a1}$ can be found from:

$$V0_{a1} = -\left(\frac{R3_{a1}}{R2_{a1}}V1_{amp1} + \frac{R3_{a1}}{R4_{a1}}V_{ac}\right) \quad (26)$$

$V0_{a1}$ becomes

$$V0_{a1} = -1V1_{amp1} - 0.5V_{ac} = -(-V_{ac}) - 0.5V_{ac} = V_{ac} \text{for } V_{ac} \geq 0 \quad (27)$$

During interval 2 (negative half-cycle), V_{ac} is negative, and $V2_{amp2} = 0$. Thus, by using Equation (26) again and if $R3_{a1} = R4_{a1} = 2R$ and $R2_{a1} = R$, $V0_{a1}$ of op-amp $A2_{a1}$ is:

$$V0_{a1} = -1V1_{amp1} - 0.5V_{ac} = -2(0) - V_{ac} = -V_{ac} \text{for } V_{ac} < 0 \quad (28)$$

Next, stage 3 presents the input reference signal for the CCL. The AC supply is used as a reference signal represented as reference current I_{ref}. The magnitude of I_{ref} is determined based on the peak amplitude of the distorted supply current waveform, which is derived from the rectifier's operation devoid of any filtering mechanism.

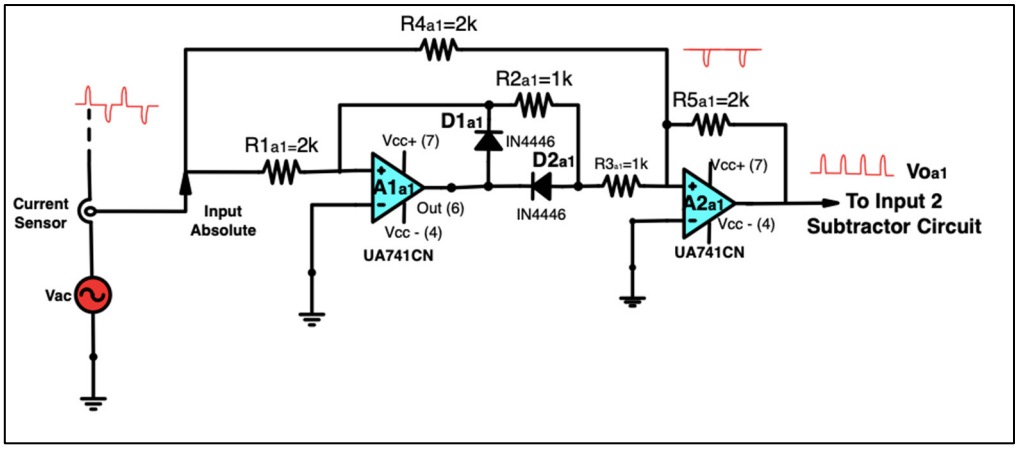


Figure 16. Absolute circuit of CCL.

Stage 4 performs similarly to stage 2, in which the bipolar form of the reference signal is converted to the unipolar form. The output from the operational amplifier is a positive voltage indicative of the absolute magnitude of the input reference signal, regardless of its initial positive or negative value.

In stage 5, the output of the subtractor circuit is presented as shown in Figure 17. The subtractor circuit is used to subtract the sensed supply current (distorted current) I_{dist} with I_{ref}, in order to produce an error signal. This error signal needs to be eliminated for improving the supply current to be without distortion.

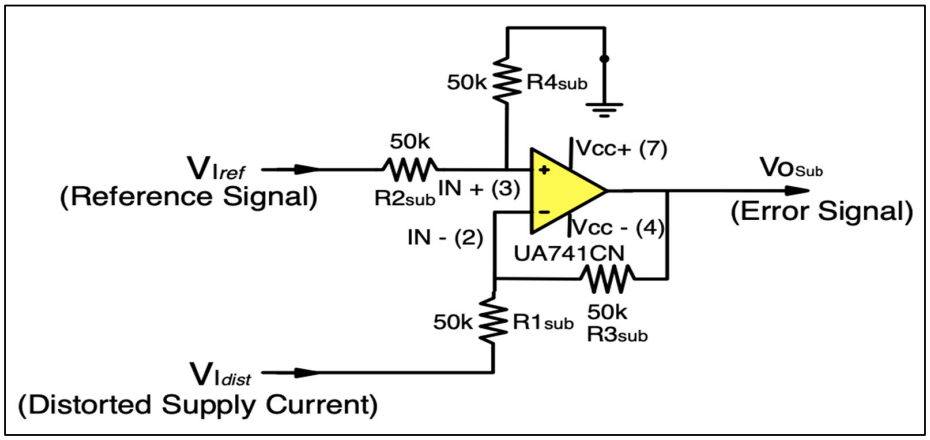


Figure 17. Schematic diagram of subtractor circuit.

The effect of subtraction can be seen from the following qualitative observations. If V_{Idist} = 0, then R1sub becomes grounded and V_p is proportional V_{Iref}, and so we have a non-inverting amplifier with Vo_{sub} proportional to $V2_{sub}$. However, if V_{Iref} = 0, then V_p = 0, and so we have an inverting amplifier with Vo_{sub} proportional to $-V1sub$. Thus, in general we expect the output to be different voltage.

For a quantitative analysis, the op-amp is assumed to be ideal and note that $R2_{sub}$ and $R3_{sub}$ form a voltage divider such that

$$V_P = \frac{R3_{sub} V2_{sub}}{R2_{sub} + R3_{sub}} \tag{29}$$

Then, since an ideal op-amp has

$$\begin{gathered} Vin(2) = Vin(3) = Vpandin = 0, \\ i_3 = -i_1 = -\frac{V_{Idist} - V_{in(2)}}{R1_{sub}} = \frac{R3_{sub}}{R2_{sub}+R3_{sub}}\left(\frac{V_{Iref}}{R1_{sub}}\right) - \frac{V_{Idist}}{R1_{sub}} \end{gathered} \tag{30}$$

Therefore,

$$\begin{aligned} Vo_{sub} = V_{in(2)} + R3_{sub} i_3 &= \frac{R3_{sub}}{R2_{sub}+R3_{sub}} V2_{sub} + \frac{R3_{sub}}{R2_{sub}+R3_{sub}}\left(\frac{R3_{sub}}{R1_{sub}}\right) V2_{sub} - \frac{R3_{sub}}{R1_{sub}} V_{Idist} \\ &= \frac{R3_{sub}}{R1_{sub}}\left(\frac{1+\frac{R1_{sub}}{R3_{sub}}}{1+\frac{R2_{sub}}{R3_{sub}}}\right) V_{Iref} - \frac{R3_{sub}}{R1_{sub}} V1_{sub} \end{aligned} \tag{31}$$

Finally, if $\frac{R2_{sub}}{R3_{sub}} = \frac{R1_{sub}}{R3_{sub}}$, then

$$Vo_{sub} = \left(\frac{R3_{sub}}{R1_{sub}}\right)(V2_{sub} - V1_{sub}) \tag{32}$$

Stage 6 presents the PI controller, as shown in Figure 18. With a proper tuning of proportional gain K_p and the integral gain K_i, the error signal as discussed in stage 5 can be eliminated. For this purpose, the two variable resistors R_p and R_i are used to vary the amplitude of the error signal. First, R_p is set to 80 kΩ to get K_p of 8. Then, R_i is set to 400 kΩ to get K_i of 27. The error from the output of the subtractor circuit is the input to the proportional controller.

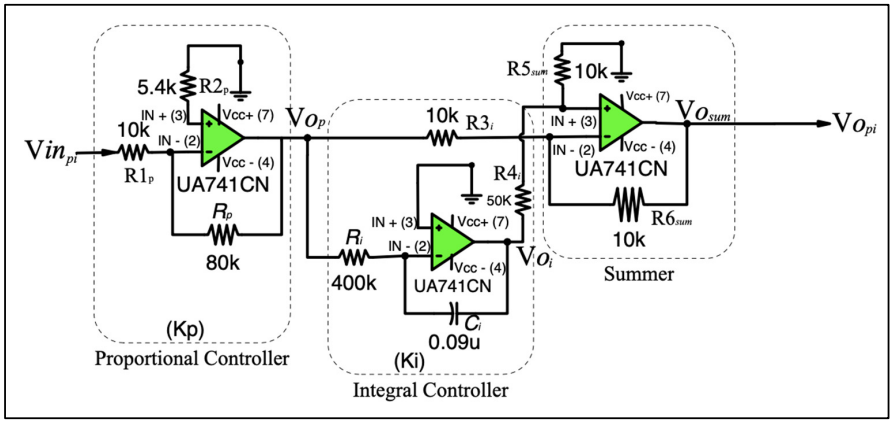


Figure 18. PI controller circuit.

Meanwhile, two important notes must be taken. First, the output of proportional controller is inverted. Also, it has no offset. The input to the integral controller is the output of the proportional controller, or is defined as below:

$$Vin_{pi} = -K_p V_{error} \tag{33}$$

With initial condition of Vo_i, the output of the integral controller is

$$\begin{aligned} Vo_i &= -\tfrac{1}{R_iC_i}\int Vin_{pi}dt + Vo_p \\ &= -K_i\int Vin_{pi}dt + Vo_p \end{aligned} \quad (34)$$

Substituting $Vin_{pi} = -K_pV_{error}$ into Equation (34) gives

$$\begin{aligned} Vo_i &= -K_i\int \left(-K_pV_{error}\right)dt + Vo_p \\ Vo_i &= K_pK_i\int \left(V_{error}\right)dt + Vo_p \end{aligned} \quad (35)$$

The summer is actually a different amplifier, or can be defined as below:

$$\begin{aligned} Vo_{sum} &= \tfrac{10k}{10k}\left[\left(K_pK_i\int V_{error}dt + Vo_p\right)^{-}K_pV_{error}\right) \\ Vo_{sum} &= K_pV_{error} + K_pK_i\int \left(V_{error}\right)dt + Vo_p \end{aligned} \quad (36)$$

The Laplace transform of Equation (34) is

$$Vo_{sum} = K_pV_{error} + \frac{K_pK_i}{s}V_{error}$$

By rearranging it,

$$\frac{Vo_{sum}}{V_{error}} = K_p\frac{s+K_i}{s} = K_p\frac{T_is+1}{T_is} \quad (37)$$

where

$$T_i = \frac{1}{K_i} = R_iC_i$$

If R_i = 400 kΩ and C_i = 0.09 μF,

$$K_i = \frac{1}{R_iC_i} = \frac{1}{(400k)(0.09\mu)} = 27$$

Stage 7 represents the triangular carrier signal. The 10 kHz triangular carrier signal is used to represent the switching frequency of the APF.

In stage 8, the comparator circuit is used to generate the asynchronous PWM (APWM) signal by comparing the triangular carrier signal with the output signal of the PI controller. This APWM signal is used to control switches S3a and S1b for charging and discharging of boost inductor to perform the APF function.

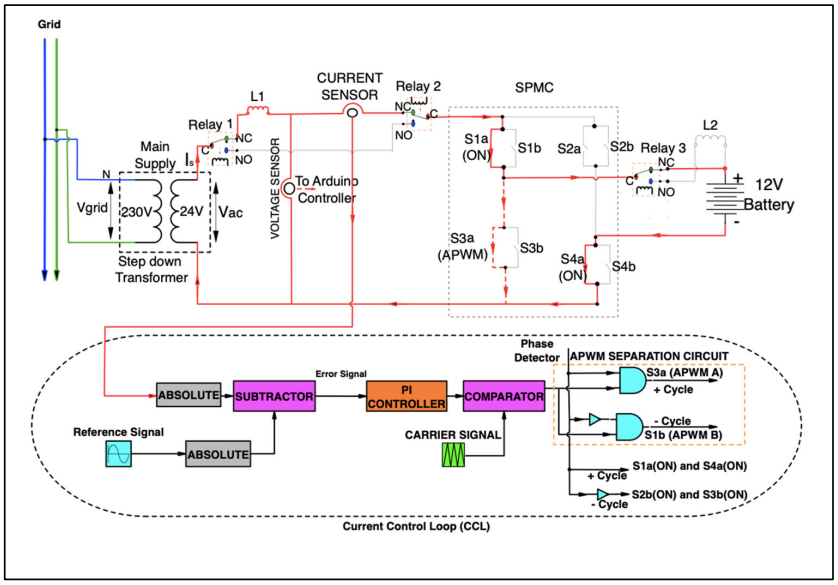
Finally, in stage 9, the APWM separation circuit is developed for positive and negative cycle operations, by using two gates, an AND gate and an inverter gate. The separation is performed by comparing the generated APWM signal with the phase detector signal. The positive cycle is used to control S3a, while the negative the cycle is used to control S1b.

As mentioned in Section 1, the preliminary assessment was performed on the previous switching strategy in [23]. The switching strategy was implemented in the experimental work. However, the initial findings showed the output voltage of inverter operation was lower than expected with only 8 V. The designed target should be to producing at least 24 V in order for it to be possible to step the voltage up to 230 V using the step-up transformer connected to the grid. In addition, the boost inverter was used to boost output voltage, which, however, could only rise to 12 V. Therefore, further improvement to the switching algorithm is proposed, as detailed in the next subsections. The next subsections will explain the operation of the proposed UPS system in two designed modes: controlled rectifier (charging mode) and controlled inverter (discharging mode).

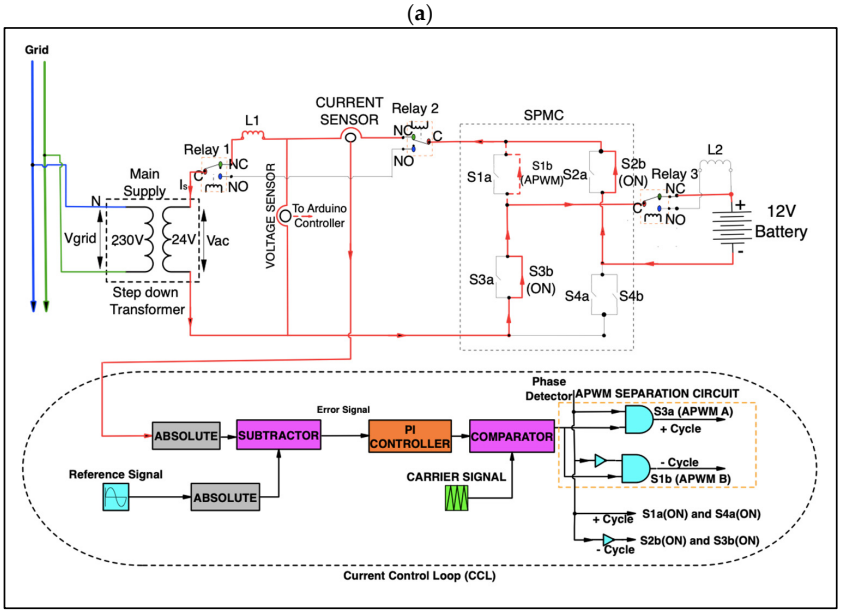
4.2. Controlled Rectifier Mode (Charging Mode)

The function of the controlled rectifier mode, also known as the charging mode, is to facilitate the conversion of AC from the grid to the DC required by the load [24,30]. This conversion process, when integrated with APF capabilities, involves two distinct operational phases: the positive and negative cycles. The APF's role is pivotal in enhancing the quality of the supply current waveform, transforming it into a continuous, sinusoidal form

that is synchronized with the supply voltage waveform. This adjustment significantly diminishes the THD and augments the power factor. Figure 19 elucidates the comprehensive mechanism of the controlled rectifier mode, whereas Table 3 details the specific switching strategy employed for both the positive and negative cycles. An in-depth exploration of each cycle's operation is provided below.



(**a**)



(**b**)

Figure 19. Schematic diagram of controlled rectifier mode in UPS: (**a**) positive and (**b**) negative cycles.

Step 1 (Positive Cycle):

During the positive cycle, the inductor L1 initiates energy accumulation as switches S1a and S3a remain activated and turned ON. S3a's operation is modulated by the APWM signal emanating from the CCL.

Step 2 (Positive Cycle):

Subsequently, as L1 transitions to the de-energization phase, the previously accumulated energy is relayed to capacitor C1, with switches S1a and S4a maintaining their active turned ON states to ensure a continuous flow of supply current.

Step 3 (Negative Cycle):

Conversely, in the negative cycle, the energization of L1 commences with the activation of switches S3b turned ON and S1b APWM Signal. The flow of supply current through S1b is governed by the APWM signal from the CCL. In this mode of operation, the line inductor (L1) starts charging the energy base on the APWM pulse signal when the pair of switches S3b and S1b are turned ON.

Step 4 (Negative Cycle):

In this negative cycle, consistently activated S3b turned ON, leads to the subsequent de-energization phase of L1. During this phase, the energy stored is dispensed to the resistive-capacitive (RC) load, facilitated by the continuous activation of switches S3b and S2b. The graphical representation of the waveforms pertaining to the charging mode is depicted in Figure 23, with the mode's operation spanning from 0 to 40 ms.

Table 3. Switching strategy for rectifier operation.

Switch	Rectifier Mode	
	Positive Cycle	**Negative Cycle**
S1a	ON	Off
S1b	Off	APWM
S2a	Off	Off
S2b	Off	ON
S3a	APWM	Off
S3b	Off	ON
S4a	ON	Off
S4b	Off	Off

4.3. Managed Inverter Phase (Energy Release Mode)

The functionality of the managed inverter phase (energy release mode) pertains to the transformation of DC to AC, facilitating the conversion of DC energy from a backup source into the AC format necessary for the load [22,30]. Utilizing a boost inverter for the DC to AC conversion process, this mode produces an AC output voltage that exceeds the initial DC input; this elevation in output voltage is achieved through the modulation index of SPWMs. The switching frequency of 5 kHz will generate signals of 50 pulses for half a cycle and 100 pulses for one full cycle. Therefore, to generate the SPWM signal by using the Arduino Uno controller, the time of the pulse signals is required. Thus, the sampling time for the half-cycle of the 5 kHz SPWM signal is captured from MATLAB/Simulink. The details of sampling time for the 5-kHz SPWM signal with the modulation index of 0.5 are presented in Appendix A. The Switching frequency is set to 5 kHz for experimental dan simulation test base on the previous work published in [31].

The input voltage of 12 V from a battery incorporated with a boost inductor of 2 mH is used to develop an output AC voltage of 24 V. The voltage level is enough to send it back to the grid via a 24/230 V step up transformer. During power outage condition, the voltage sensor senses the value of the supply voltage level as zero. The UPS operation automatically changed from charging mode to discharging mode. As previously highlighted, a switching strategy was devised to guarantee the generation of a minimum output voltage of 24 V, facilitating the amplification of voltage to 230 V via a step-up transformer for grid integration. This aspect of the research has been meticulously focused on the switching technique within the managed inverter phase, ensuring its practical applicability for experimental validation on a test rig.

Figure 20 delineates the comprehensive mechanism of the managed inverter phase, incorporating a safe-commutation feature alongside innovative switching strategies for both the positive and negative cycles. Concurrently, Table 4 outlines the specified switching strategy and pulse signals designated for each cycle. An expanded explanation for the operational dynamics of each cycle is provided.

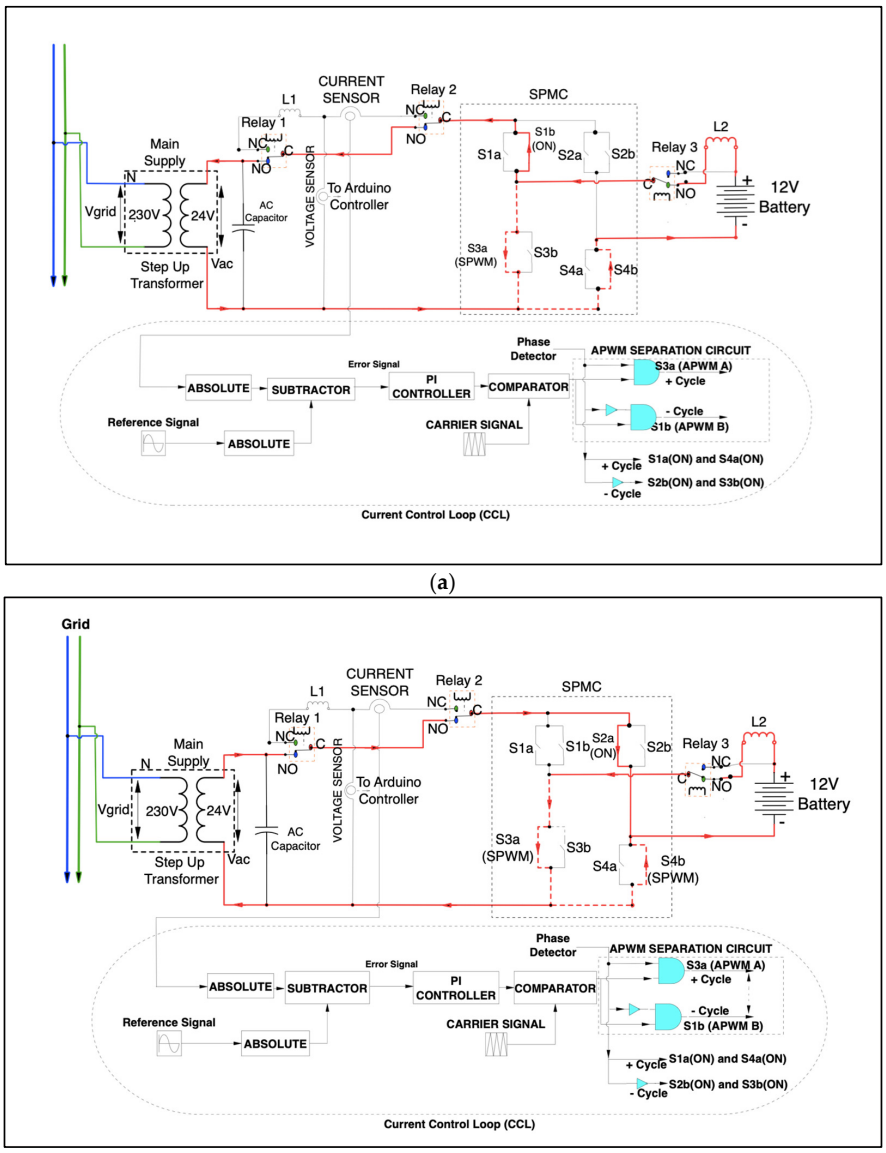


Figure 20. Schematic diagram of controlled inverter mode in UPS: (**a**) positive and (**b**) negative cycles.

Table 4. Switching algorithm of inverter operation mode for UPS system.

Inverter Operation	Positive Cycle		Negative Cycle	
	Switching	**Starting Pulse**	**Switching**	**Starting Pulse**
S1a	Off	Off	Off	Off
S1b	ON	High	Off	Off
S2a	Off	Off	ON	High
S2b	Off	Off	Off	Off
S3a	SPWM	Low	SPWM	High
S3b	Off	Off	Off	Off
S4a	Off	Off	Off	Off
S4b	SPWM	Low	SPWM	High

Positive cycle:

Step 1: For the positive cycle operation, the Arduino Uno controller generates the 1st to 50th pulses of the SPWM signal. As shown in Figure 21, for S3a, the 1st pulse is

generated after a delay time (OFF state) of 97 µs, then the ON state of 6 µs, before it turns to the OFF state for 188 µs. The process is continuous until the Arduino Uno controller generates the 50th pulse as illustrated in Figure 22. Figure 22 illustrates generation of the SPWM signal using the Arduino Uno controller based on the sampling time as tabulated in Appendix A.

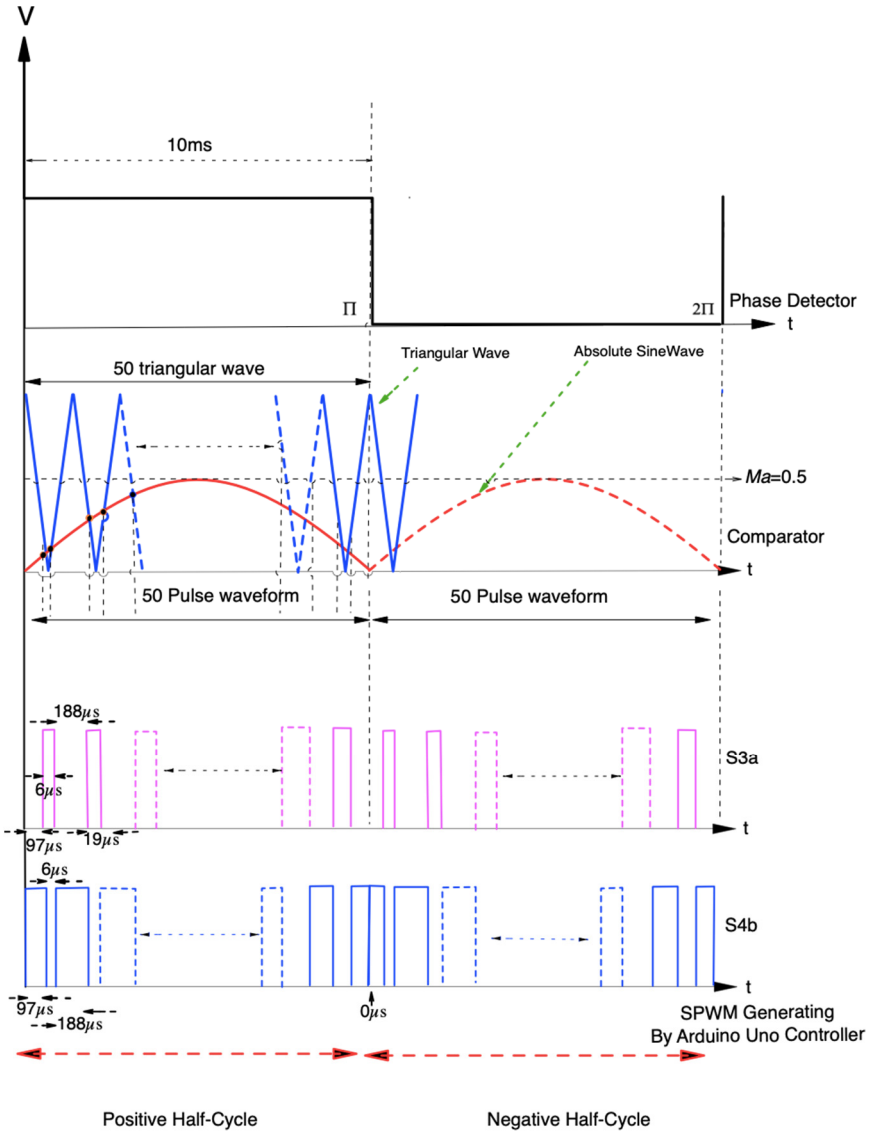


Figure 21. Generation of SPWM signal for half-, positive, and negative cycles by using Arduino Uno Controller.

For S4b, the 1st pulse is generated to be the ON state of 97 µs, then the OFF state of 6 µs, before it turns to the ON state for 188µs. The process is continuous until the Arduino Uno controller generates the 50th pulse as illustrated in Figure 22.

Step 2: Energy is stored in the boost inductor as current flows from the 12V battery supply through the combination of switches S3a and S4b.

Step 3: Subsequently, the energy previously accumulated is conveyed to the load via the switch pair S1b and S4b, marking the transition of DC power to the AC load during the positive half-cycle of the boost inverter operation. To facilitate this process, switch S1b is activated to the 'ON' position, whereas switches S3a and S4b are modulated by the SPWM signal, employing a modulation index set at 0.5.

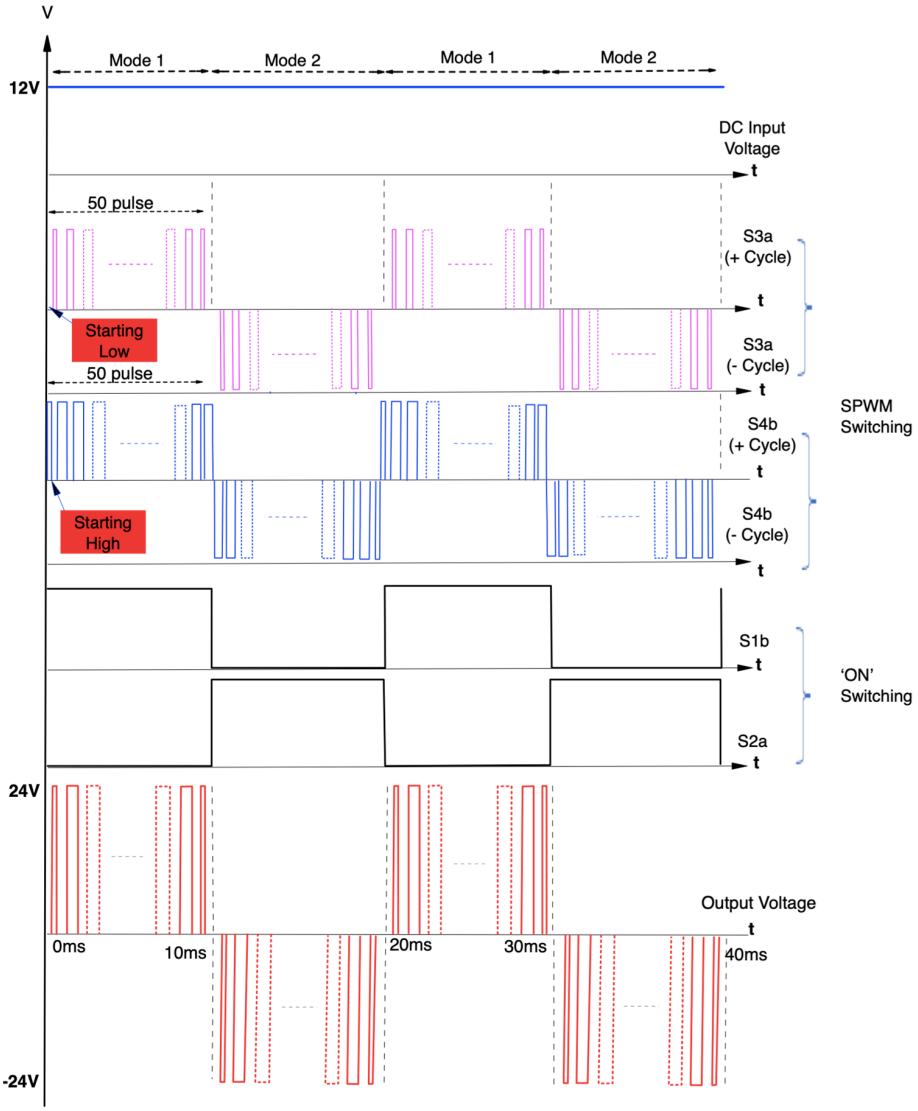


Figure 22. Waveform pattern of switching pulse for the controlled inverter with boost operation.

Negative cycle:

Step 1: For the negative cycle operation, the Arduino Uno controller generates the 51st to 100th pulses. The generation of SPWM signal for this cycle is also shown Figure 18 and Appendix A. For S3a, the 51st pulse is generated after a delay time (OFF state) of 199 µs, then the ON state of 2 µs, before it turns to the OFF state for 197 µs. The process is continuous until the 100th pulse as also illustrated in Figure 22.

For S4b, the 51st pulse in this cycle is generated to be ON state of 199 µs, then the OFF state of 2 µs, before turning to the ON state for 197 µs. The process is continuous until the the 100th pulse is generated.

Step 2: The configuration of the SPWM is designated as step 1, wherein switch S1b is deactivated, and the duo of S3a and S4b remains under the regulation of the SPWM, also in accordance with step 1. During this phase, the initiation of the SPWM signal is characterized by a high pulse pattern, specifically tailored for the negative half-cycle.

Step 3: During this phase, current is drawn from the 12V battery supply and directed towards the AC load via S3a, then returns through S2a. Consequently, this facilitates the conversion of DC power to the AC load, executing the boost function of the inverter throughout the negative half-cycle.

The waveforms of the discharging mode are shown in Figure 23, operating after the charging mode. The period assigned for this mode is from 40 to 80 ms.

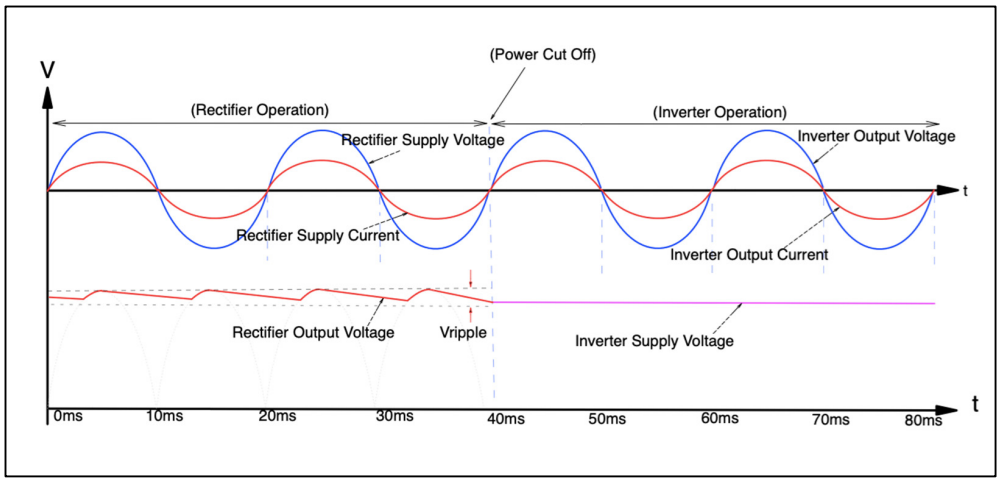


Figure 23. The waveforms of charging (rectifier operation) and discharging (inverter operation) modes.

5. Simulation Model and Experimental Test Rig

The developed UPS system, based on the SPMC topology, was subjected to simulation within the MATLAB/Simulink environment. As delineated in the preceding discussion, the adoption of a novel switching strategy is pivotal for amalgamating the functionalities of both the rectifier and the inverter, as detailed in Tables 3 and 4. The specifications for the UPS under consideration are itemized in Table 5, with parameter values aligned with those typically encountered in UPS systems, referencing [24,32–35].

Table 5. Parameters for experimental test rig.

Parameter	Value
AC supply voltage, *Vac*	24 V
DC supply voltage, *Vdc*	12 V
Boost inductor, *Ls*	2 mH
Inductor load, L_L	5 mH
Capacitor load, *CL*	1000 µF
Resistive load, *RL*	300 Ω
Switching frequency for rectifier, *fs*	10 kHz
Switching frequency for inverter, *fs*	5 kHz
Proportional gain, *Kp*	8
Integral gain, *Ki*	27

Figure 24 delineates the circuit's three primary components of the proposed UPS configuration. In this analysis, a step response methodology is employed to assess the transition duration between the rectifier and inverter phases. Specifically, the rectifier phase is analysed over a sample period from 0 to 0.04 s, while the inverter phase spans from 0.04 to 0.08 s.

To facilitate seamless transitions at t = 0.04 s, a pair of breaker switches are strategically implemented to concurrently manage the supply and load functionalities, as depicted in Figure 24. In the charging phase, from 0 to 0.04 s, the rectifier signal breaker (B) is activated, whereas the inverter signal breaker (A) is deactivated. The shift to inverter operation is initiated at t = 0.04 s, during which B is deactivated, and A is activated, ensuring a smooth transition between operational modes.

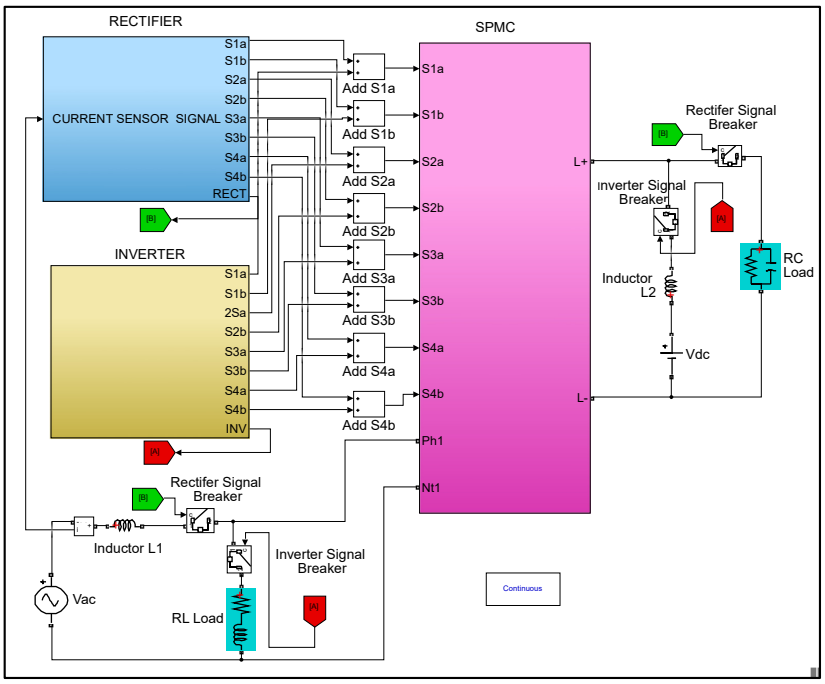


Figure 24. Three main blocks of the proposed UPS.

In the experimental work, the proposed UPS using SPMC topology was constructed and tested to validate its performance as done in the simulation. In this work, a 24 V AC supply is used to produce at least 15 V output DC voltage to charge a 12 V battery. The 12 V RS 698-8091 Pro Lead-acid batteries are used, which are also well known across several industries and for general purposes. The battery is sealed and ideal for use in UPS and emergency back-up [32].

In the first stage, the Arduino UNO controller is programmed to generate 5-kHz PWM signal to control the SPMC circuit to investigate operation of the controlled rectifier. Further construction has been developed for the controlled rectifier operation using RC load to represent the non-linear load without and with the APF function as shown in Figure 25. This work uses a 10 kHz switching frequency to generate an APWM signal [36].

Next, in the second stage, the construction and implementation of the experimental test rig are continued with the controlled inverter operation as shown in Figure 26. The 12V DC supply from the battery is used in this work, as discussed in the previous subsection. The 5-kHz SPWM signal is used to control the SPMC. The construction and implementation of the controlled inverter are using R and RL loads without and with safe-commutation strategy.

The third stage presents the construction and implementation of the proposed UPS system, as it full schematic diagram is shown in Figure 27. Meanwhile, the experimental test rig is shown in Figure 28.

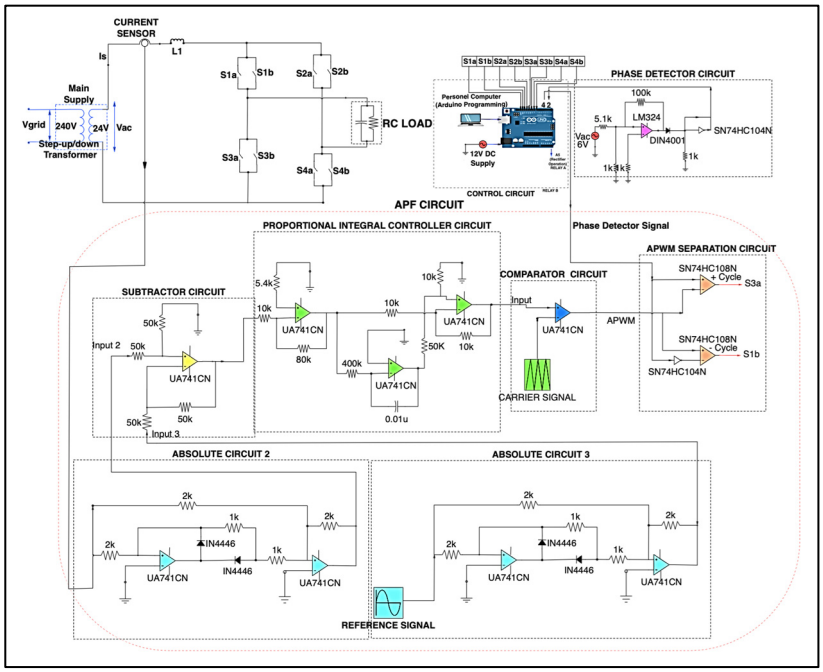


Figure 25. Schematic diagram of controlled rectifier incorporated with APF function.

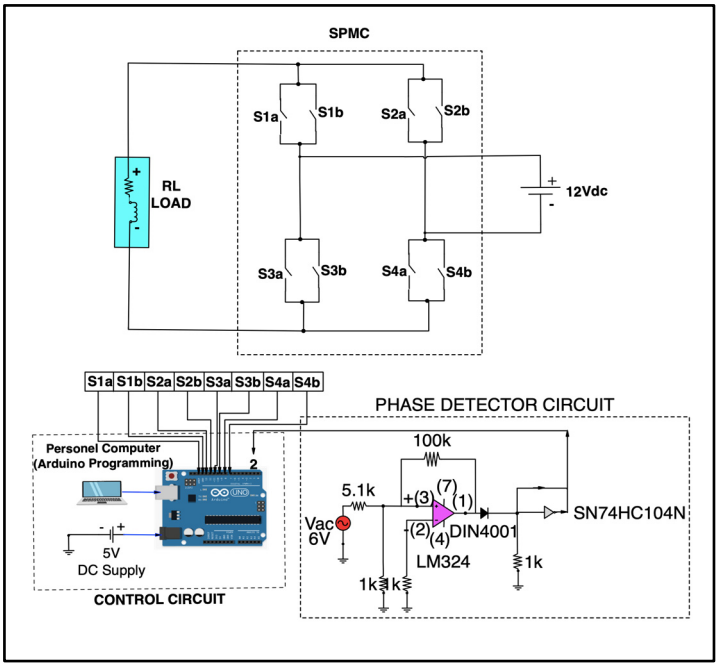


Figure 26. Schematic diagram of controlled inverter operation.

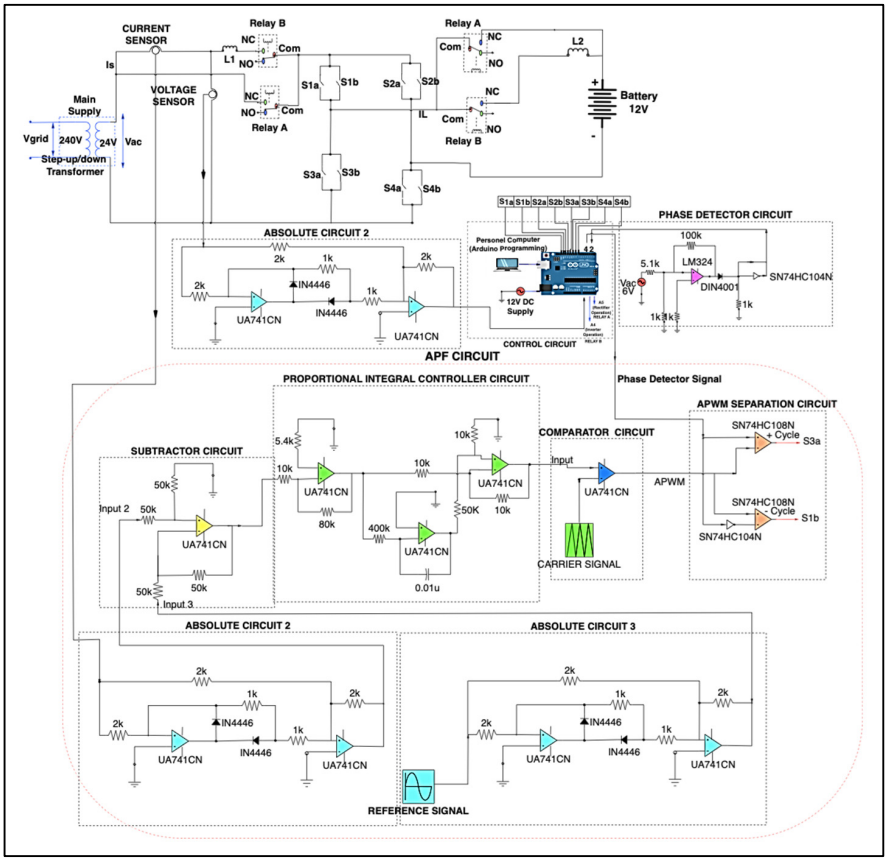


Figure 27. Full schematic diagram of UPS system.

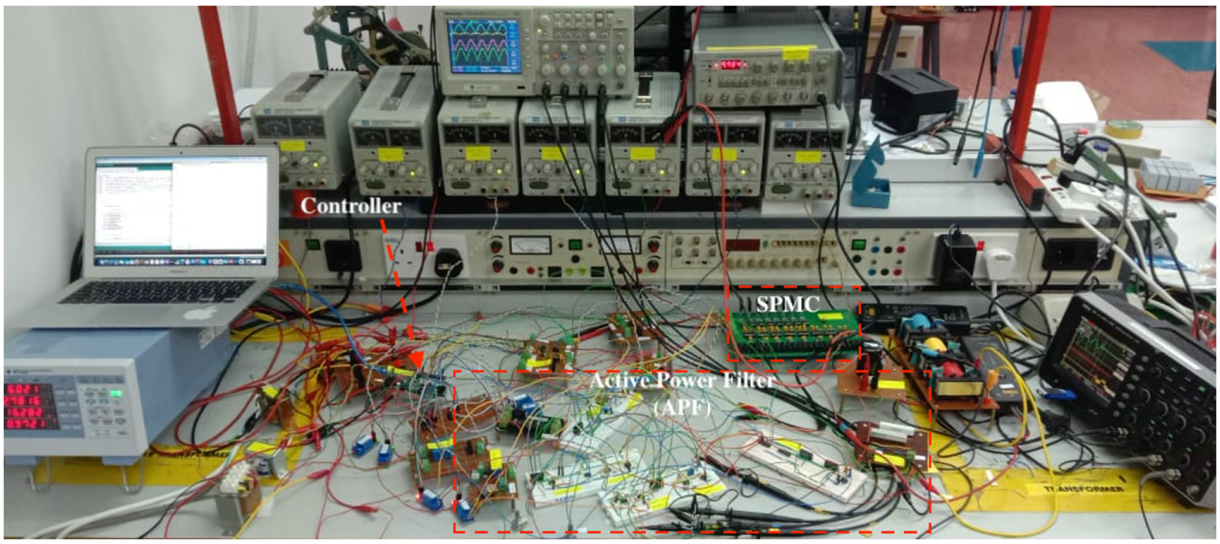


Figure 28. Experimental test rig for the proposed UPS system.

6. Results

Figure 29 presents the experimental test rig results for the supply current and voltage waveforms using a controlled rectifier with a non-linear load, without the active power filter (APF) function. The results indicate a misalignment and distortion between the supply current and voltage, leading to high total harmonic distortion (THD) levels and reduced efficiency. This distortion adversely affects the supply current waveform, resulting in associated issues such as poor overall power factor, heating effects, device malfunction, and potential damage to other equipment due to nonlinear loads.

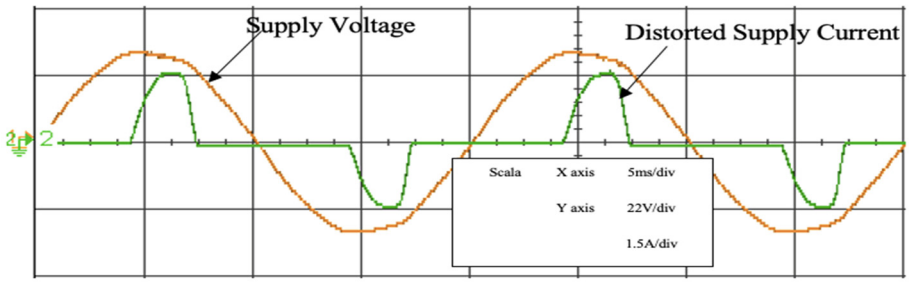


Figure 29. Experimental findings for supply current and voltage utilizing the controlled rectifier devoid of APF.

The harmonic content of the distorted supply current waveform, as determined through both simulation and experimental means, is showcased in Figures 30 and 31, benchmarked against the IEEE 519-2022 standard [37]. The THD percentages recorded were 189.85% for the simulation and 114.65% for the experimental setup, both exceeding the prescribed standards. These elevated THD levels corroborate prior findings regarding significant harmonic presence, as introduced in Section 1, indicating severe distortion in the supply current that could lead to reduced power factor, overheating, equipment malfunction, and damage.

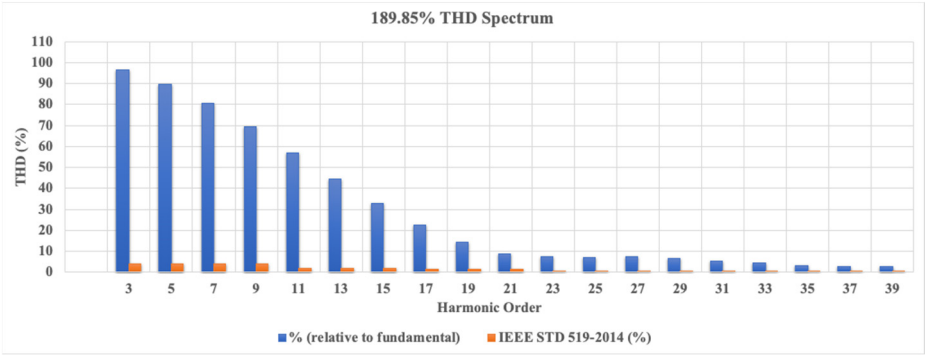


Figure 30. Harmonic distribution of the distorted supply current derived from simulation data of the controlled rectifier lacking APF.

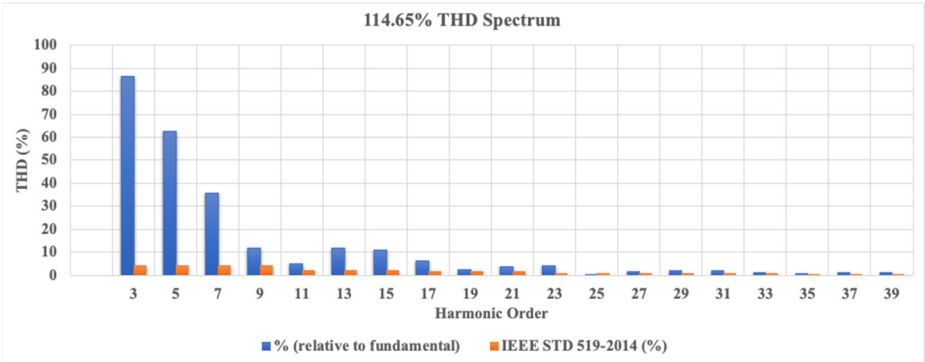


Figure 31. Harmonic profile of the distorted supply current from experimental observations of the controlled rectifier without APF.

Comparative analysis of the supply current and voltage for the controlled rectifier equipped with APF functionality is presented in Figures 32 and 33, showing successful harmonic compensation. In the charging mode of operation, the UPS operates with APF function consisting of the absolute circuit for supply distorted current and reference signal, subtractor circuit, PI controller circuit, comparator circuit, and APWM separation circuit to compensate for the distorted supply current waveform to become continuous, sinusoidal

and in phase with the supply voltage waveform resulting in high power factor and low THD level.

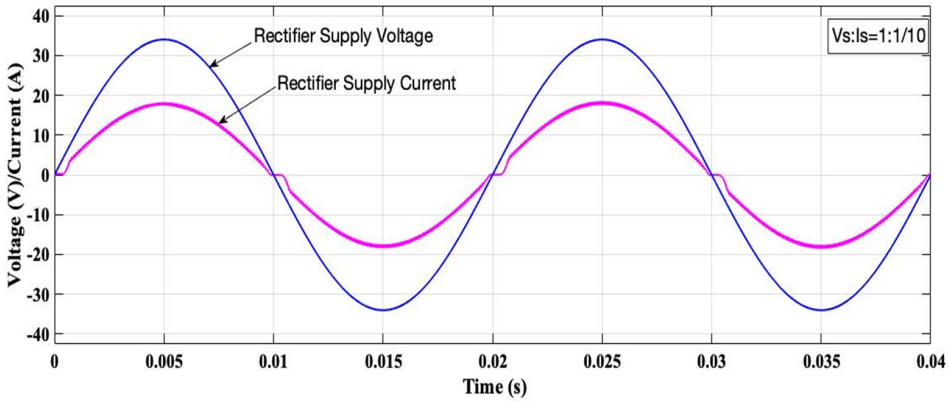


Figure 32. Simulation findings for supply current and voltage using the controlled rectifier equipped with APF.

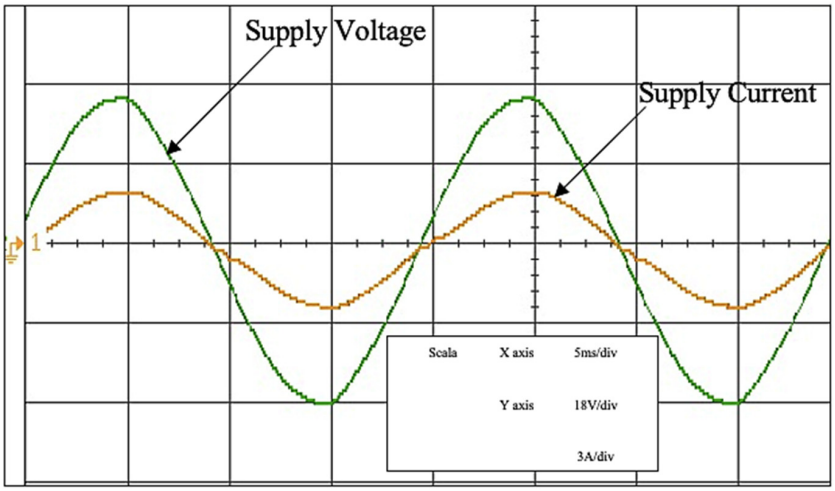


Figure 33. Experimental outcomes for supply current and voltage from the controlled rectifier integrated with APF.

Further, Figures 34 and 35 display the harmonic spectrum and THD levels for the supply current, adhering to the IEEE 519-2022 Standard, from both simulation and experimental evaluations. THD percentages were found to be significantly lower at 3.59% and 7.81%, respectively, indicating compliance with the standard.

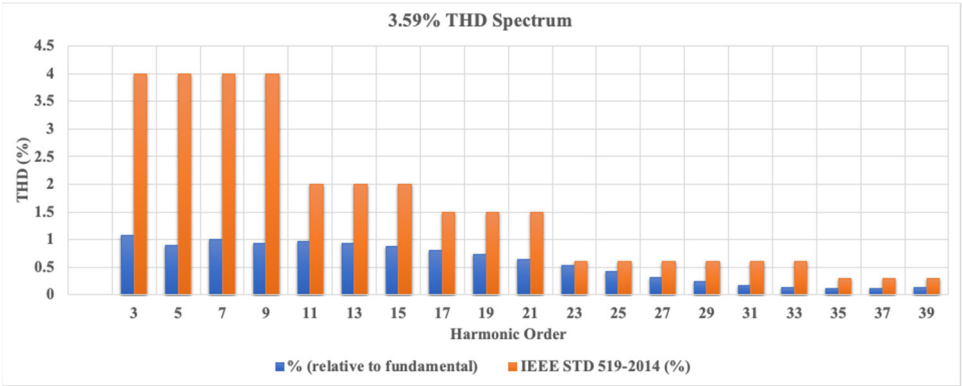


Figure 34. Harmonic analysis of the supply current from simulation data of the controlled rectifier incorporating APF.

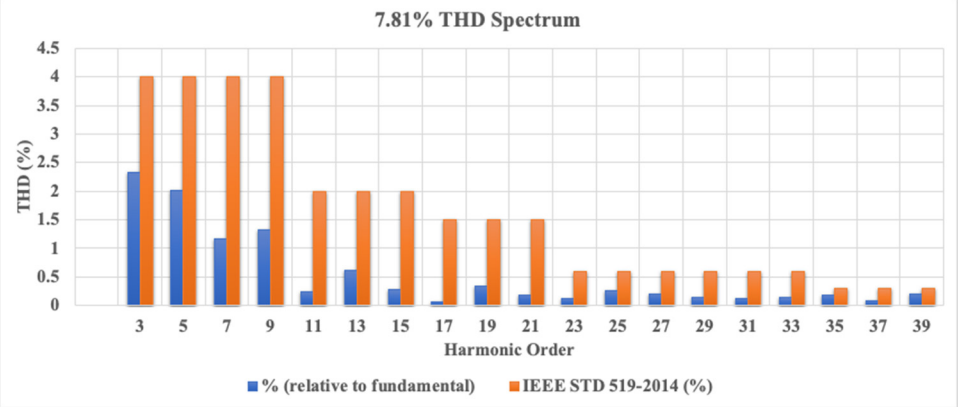


Figure 35. Harmonic profile of the supply current derived from experimental findings of the controlled rectifier with APF.

The proposed switching strategy for a controlled boost inverter with a passive filter has demonstrated its efficacy in successfully generating the desired output voltage suitable for grid supply. As evidenced in Figures 36 and 37, the inverter effectively boosts the input voltage of 12 V DC from a battery to generate an output AC voltage of 38 V. This output voltage is sufficient for a transformer to step up the voltage to 415 V AC, which is the required level for grid integration.

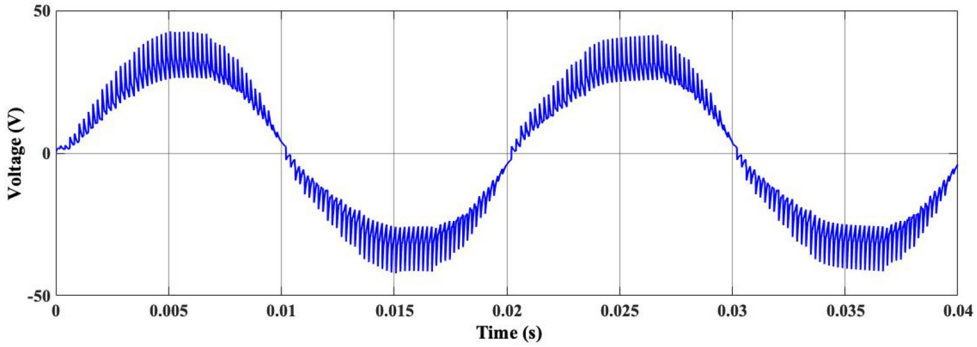


Figure 36. Simulation outcomes for the output voltage of the controlled boost inverter equipped with a passive filter.

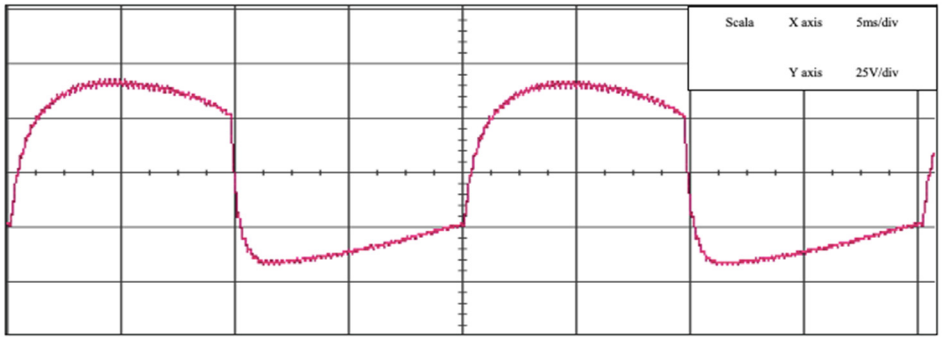


Figure 37. Experimental findings for the output voltage from the controlled boost inverter using a passive filter.

Additionally, Figure 38 presents the simulation outcomes for the UPS system's supply voltage during both charging and discharging phases, utilizing the developed switching algorithm and a step response block to manage transition timing. Operational timings were defined as 0 to 0.04 s for charging and 0.04 to 0.08 s for discharging, aiming to assess the system's operational fluidity.

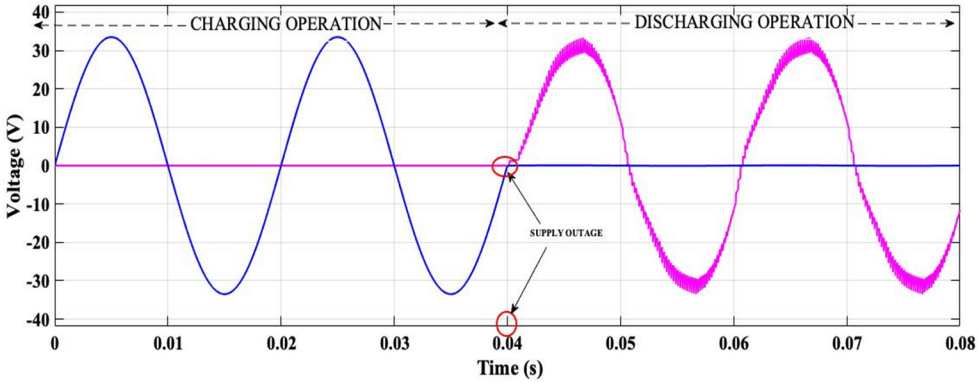


Figure 38. Simulation outcomes depicting the supply voltage waveform in charging mode and the output voltage waveform in discharging mode.

Experimental validations are further extended, as shown in Figure 39, which illustrates the supply voltage and current during the UPS system's charging and discharging modes, demonstrating a harmonious correlation between simulation and experimental data. The transitions between modes were smooth, indicating the controller's effectiveness in adapting to operational shifts. Notably, the supply current exhibited a sinusoidal form, aligning with the supply voltage, thereby reducing THD levels and enhancing power factor. Simulation results indicated a THD level of 6.59% and a power factor of 0.9996, whereas experimental findings reported a THD of 7.86% and a power factor of 0.9715, as measured by a YOKOGAWA WT333E Digital Power Meter (Yokogawa Test & Measurement Corporation, Tokyo, Japan).

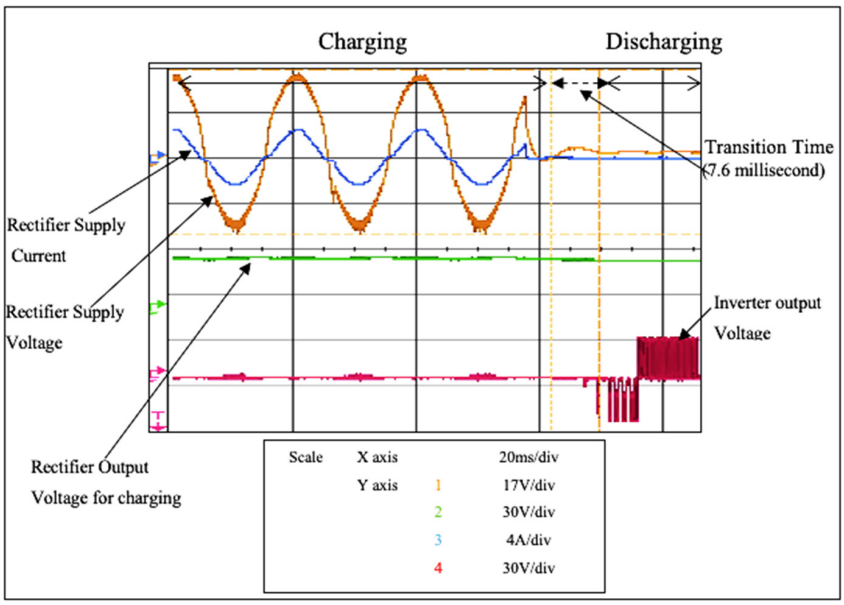


Figure 39. Experimental findings illustrating the waveform of supply voltage during charging mode and the waveform of output voltage during discharging mode.

Comparisons of harmonic spectra against the IEEE 519-2022 standard in Figures 40 and 41 confirm that the harmonic levels are within acceptable limits and meet the standard's requirements. Table 6 consolidates the comparative outcomes for the simulation and experimental setups, both with and without APF functionality, underscoring the APF's role in diminishing THD levels and improving power factor. The observed discrepancy in THD levels between the simulation and experimental setups can be attributed to the inductive effects of the step-down transformer windings, highlighting the APF function's critical impact on reducing THD when combined with a suitably designed switching algorithm.

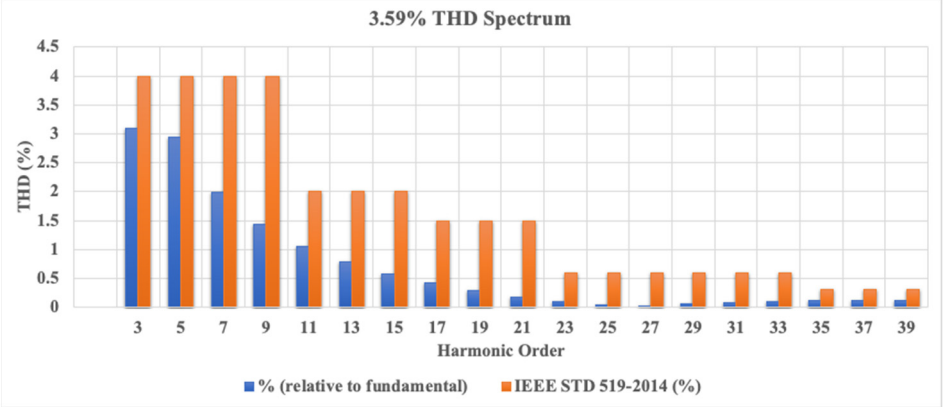


Figure 40. Harmonic analysis of the supply current derived from simulation data for the controlled inverter integrated with APF.

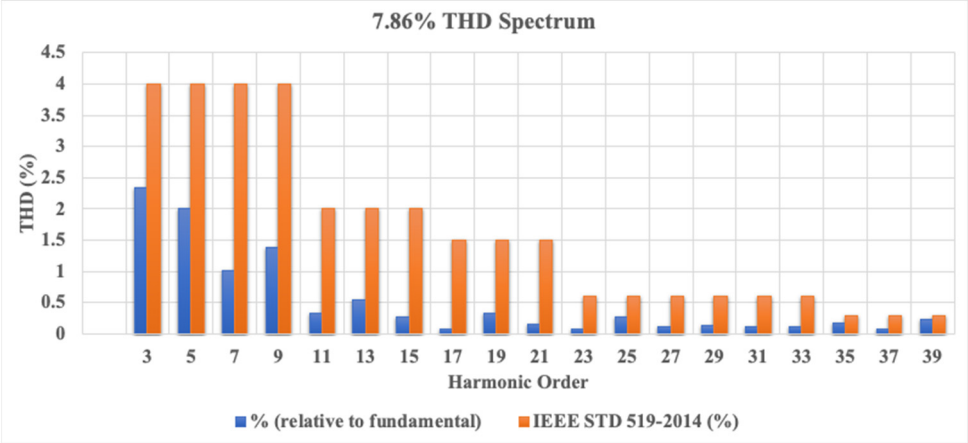


Figure 41. Harmonic distribution of the supply current from experimental outcomes for the controlled inverter equipped with APF.

Table 6. Performance Comparison of Simulation and Experimental Test rig.

Strategies		THD (%)	Power Factor (pf)
Rectifier without APF	Simulation	189.85	0.6248
	Experimental test rig	114.65	0.6391
Rectifier with APF	Simulation	3.59	0.9996
	Experimental test rig	7.81	0.9725
UPS with APF	Simulation	3.59	0.9996
	Experimental test rig	7.86	0.9715

7. Conclusions

This paper elaborates on the effective deployment of a UPS system utilizing SPMC circuit architecture, enhanced with APF capabilities. The designed UPS, an integrated SPMC unit, is adept at fulfilling both rectifying and inverting functions, potentially obviating the need for separate rectifier and inverter circuits found in traditional UPS configurations. The investigation encompassed the UPS's performance in both charging (rectifier) and discharging (inverter) modes. Furthermore, the incorporation of APF functionality through a boost technique effectively mitigates the fluctuations in the supply current waveform, rendering it continuous, sinusoidal, and synchronized with the supply voltage waveform, thereby elevating the power supply system's quality. Consequently, the THD of the supply current was significantly diminished to levels below those stipulated by the IEEE519-2022 standard. Moreover, the transition duration between the UPS's charging

and discharging modes aligns with the specifications of the IEC62040-3 standard [38]. This study's paramount contribution lies in advancing UPS design UPS using SPMC topology, which could be extended for development of various advanced applications such as wireless power charging, fast and high-density micro charging, micro UPS, etc. This is in line with the rapidly evolving global manufacturing landscape that calls for high quality and availability of power supply and can contribute to various applications, from electric vehicles (EVs) to biological implants such as pacemakers in medical technology industries. Future studies could engage in comparative analyses with alternative topologies, assessing higher ratings and efficiency to further endorse the proposed UPS's potential and applicability.

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Data Availability Statement: Data are contained within the article. To estimate the analyzed results, the authors used raw data from the databases included in Appendices A and B.

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Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

Table A1. Sampling Time for SPWM Generator.

No. of Pulse	Positive Cycle (μs)	No. of Pulse	Positive Cycle (μs)	No. of Pulse	Negative Cycle (μs)	No. of Pulse	Negative Cycle (μs)
1	97	26	141	51	0	76	132
2	6	27	54	52	199	77	73
3	188	28	150	53	2	78	123
4	19	29	46	54	197	79	83
5	175	30	158	55	4	80	112
6	31	31	38	56	195	81	93
7	163	32	165	57	6	82	102
8	44	33	31	58	192	83	104
9	150	34	172	59	10	84	91
10	56	35	25	60	188	85	115
11	138	36	178	61	14	86	79
12	68	37	19	62	184	87	126
13	126	38	184	63	19	88	68
14	79	39	14	64	178	89	138
15	115	40	188	65	25	90	56
16	91	41	10	66	172	91	150
17	104	42	192	67	31	92	44
18	102	43	6	68	165	93	163
19	93	44	195	69	38	94	31
20	112	45	4	70	158	95	175
21	83	46	197	71	46	96	19
22	123	47	2	72	150	97	188
23	73	48	199	73	54	98	6
24	132	49	0	74	141	99	97
25	63	50	400	75	63	100	0

Appendix B

Table A2. Experimental harmonic contents for UPS operation on RC load incorporated with APF function. Total harmonic distortion (THD) = 7.86% and power factor = 0.9715.

Frequency (Hz)	Harmonic Number	% (Relative to Fundamental)	Frequency (Hz)	Harmonic Number	% (Relative to Fundamental)
0	0	3.40	1000	20	0.13
50	1	100.00	1050	21	0.16
100	2	1.03	1100	22	0.21
150	3	2.34	1150	23	0.08
200	4	1.86	1200	24	0.26
250	5	2.01	1250	25	0.27
300	6	0.89	1300	26	0.22
350	7	1.02	1350	27	0.11
400	8	0.59	1400	28	0.14
450	9	1.39	1450	29	0.13
500	10	0.52	1500	30	0.14
550	11	0.34	1550	31	0.11
600	12	0.31	1600	32	0.21
650	13	0.54	1650	33	0.12
700	14	0.57	1700	34	0.08
750	15	0.28	1750	35	0.17
800	16	0.18	1800	36	0.09
850	17	0.07	1850	37	0.07
900	18	0.20	1900	38	0.22
950	19	0.34	1950	39	0.23

Appendix C

Table A3. Simulation result of harmonic contents for UPS Operation on RC load incorporated with APF function using MATLAB/Simulink. Total harmonic distortion (THD) = 3.59% and power factor = 0.9996.

Frequency (Hz)	Harmonic Number	% (Relative to Fundamental)	Frequency (Hz)	Harmonic Number	% (Relative to Fundamental)
0	0	0.48	1000	20	0.05
50	1	100.00	1050	21	0.63
100	2	0.13	1100	22	0.03
150	3	1.07	1150	23	0.53
200	4	0.23	1200	24	0.02
250	5	0.89	1250	25	0.42
300	6	0.12	1300	26	0.01
350	7	1.00	1350	27	0.32
400	8	0.15	1400	28	0.00
450	9	0.93	1450	29	0.24
500	10	0.13	1500	30	0.01
550	11	0.96	1550	31	0.17
600	12	0.10	1600	32	0.02
650	13	0.92	1650	33	0.13
700	14	0.10	1700	34	0.03
750	15	0.88	1750	35	0.11
800	16	0.08	1800	36	0.03
850	17	0.81	1850	37	0.12
900	18	0.06	1900	38	0.03
950	19	0.73	1950	39	0.13

Appendix D

Mathematical modeling of bidirectional switch power losses.
The average power dissipation of a semiconductor device is

$$P_{avg} = \frac{1}{T}\int_0^T p(t)dt \tag{A1}$$

where

$p(t)$ is devices instantaneous dissipated power.
T is fundamental output current period.

The power dissipation of a semiconductor device at an arbitrary time instant t is equivalent to the mean conduction and switching losses incurred within the device over the switching period $t + T_{sw}$ subsequent to t [27]. This methodology facilitates the derivation of simplified continuous time power loss expressions by approximating the instantaneous power losses as

$$P(t) \cong P_{cond}\ (t) + P_{sw}\ (t) = P_{cond}\ (t) + P_{on}\ (t) + P_{off}\ (t) \tag{A2}$$

where $P_{cond}\ (t)$ and $P_{sw}(t)$ are the average conduction losses and average switching losses at each switching period, respectively. The switching losses can be classified into two components which are turn-on losses $P_{on}\ (t)$ and turn-off losses $P_{off}\ (t)$. Turn-on and turn-off losses typically exhibit significant dissipation values in hard-switched commutation topologies, whereas soft-switched commutation results in lower dissipation values. Conversely, clocking losses are generally negligible due to the minimal leakage current of the device in its off-state. Based on the average power losses expression (A1), the total average power can be derived as follows:

$$P_{avg} \cong \frac{1}{T}\int_0^T P_{cond}(t)dt + \frac{1}{T}\int_0^T P_{on}(t)dt + \frac{1}{T}\int_0^T P_{off}(t)dt \tag{A3}$$

In this research, the UPS circuit schematic using SPMC topology is used. The analyses of power losses for the IGBT and diode are based on one IGBT (for example S1a) and one diode (for example D1b) to calculate SPMC power losses. In the general operation of SPMCs for the positive cycle, the current flows through S1a and D1b and S4a and D4b, and for negative cycle, S2a and D2b and S3a and D3b. The total average power losses of IGBTs (S1a) can be expressed as following:

$$P_{S1a}(t) \cong P_{cond/S1a}\ (t) + P_{sw/S1a}\ (t) = P_{cond/S1a}\ (t) + P_{on/S1a}\ (t) + P_{off/S1a}\ (t) \tag{A4}$$

Meanwhile, the conduction losses of IGBTs (S1a) can be expressed as below:

$$\begin{aligned} &P_{\frac{cond}{S1a}}(t) = \tfrac{1}{T_{sw}}\int_t^{t+T_{sw}} V_{S1a}(t)I_{S1a}(t)dt \\ &\cong \tfrac{1}{T_{sw}}\int_t^{t+T_{cond/S1a}} V_{S1a}(t)I_{S1a}(t)dt = V_{S1a}(t)I_{S1a}(t)dt\tfrac{T_{cond/S1a}}{T_{sw}} \\ &= V_{S1a}(t)I_{S1a}(t)D_{S1a}(t)dt \end{aligned} \tag{A5}$$

where $V_{S1a}\ (t)$ is on-state voltage of S1a and $I_{S1a}\ (t)$ can be considered to be equal to the fundamental output current $I_L\ (t)$ during the interval operation of $I_{cond/S1a}\ (t)$ if it is assumed that the cycle T_{sw} is infinitely small compared to T. Thus, several equations involved in power losses can be expressed as

$$I_{S1a}\ (t) \approx I_L(t) = I_M \sin(\omega_o t) \tag{A6}$$

$$V_{S1a}(t) = V_{t/S} + a_s I_{S1a}^{b_S} \tag{A7}$$

$$D_{S1a}(t) = \frac{1}{2}[1 + M\sin(\omega_o t + \varphi_o)] \tag{A8}$$

$$E_{on/S1a}(t) = hI^k_{S1a}(t) \tag{A9}$$

$$E_{off/S1a}(t) = mI^n_{S1a}(t) \tag{A10}$$

where

I_M is the output current amplitude.
M is the modulation depth index whose value is between 0 to 1.
ω_0 is the output frequency pulsation.

Expression (A7) has been described detail in [28]. Thus, the average conduction losses in each switching period, $P_{cond/S1a}(t)$, can be finally expressed by:

$$P_{cond/S1a}(t) \approx I_M \sin(\omega_o t)\left[V_{t/S} + a_S I^{b_s}_{S1a}\right] 0.5[1 + M\sin(\omega_o t + \varphi_o)] \tag{A11}$$

Meanwhile, switching losses of the IGBT (S1a) can also be expressed. The switching power losses are associated to the power dissipated generated during both switching transition on-off and off-on. Thus, the average turn-on losses $P_{on/S1a}(t)$ between t and $t + T_{sw}$, can be calculated as

$$\begin{aligned} P_{\frac{on}{S1a}}(t) &\approx \frac{1}{T_{sw}} \int_{t}^{t+\Delta t_{on}} V_{S1a}(t) I_{S1a}(t) dt \\ &= \frac{E_{on/S1a}(t)}{T_{sw}} = \frac{hI^k_{S1a}(t)}{T_{sw}} \end{aligned} \tag{A12}$$

The average turn-off losses switching period $P_{off/S1a}(t)$ can be expressed as

$$\begin{aligned} P_{\frac{off}{S1a}}(t) &\approx \frac{1}{T_{sw}} \int_{t+\Delta t_{on}+t_{cond/S1a}}^{t+\Delta t_{on}+t_{cond/S1a}+\Delta t_{off}} V_{S1a}(t) I_{S1a}(t) dt \\ &= \frac{E_{off/S1a}(t)}{T_{sw}} = \frac{mI^n_{S1a}(t)}{T_{sw}} \end{aligned} \tag{A13}$$

The IGBT average power losses $P_{S1a}(t)$ can be calculated by substituting expression (A6)–(A10):

$$P_{S1a}(t) = V_{S1a}(t) I_{S1a}(t) D_{S1a}(t) + \frac{E_{on/S1a}(t)}{T_{sw}} + \frac{E_{off/S1a}(t)}{T_{sw}} \tag{A14}$$

$$\begin{aligned} P_{S1a}(t) &= \left(V_{\frac{t}{S}} + a_S I^{b_S}_{S1a}\right)(I_M \sin(\omega_o t))\left(\tfrac{1}{2}[1 + M\sin(\omega_o t + \varphi_o)]\right) \\ &+ \left(\frac{hI^k_{S1a}(t)}{T_{sw}}\right) + \left(\frac{mI^n_{S1a}(t)}{T_{sw}}\right) \end{aligned} \tag{A15}$$

In analysis of diode circuits, only two primary forms of power loss merit consideration: conduction losses and turn-off losses. The turn-on and blocking losses have been omitted from this analysis due to their negligible contribution to the total power dissipation [28,29]. A detail of the D_{1b} schematic instantaneous dissipated power can be appreciated in Figure 5. Thus, $P_{D1b}(t)$ can be described as

$$P_{D1b}(t) \cong P_{cond/D1b}(t) + P_{sw/D1b}(t) = P_{cond/D1b}(t) + P_{off/D1b}(t) \tag{A16}$$

$$\begin{aligned} P_{\frac{cond}{D1b}}(t) &= \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} V_{D1b}(t) I_{D1b}(t) dt = \frac{1}{T_{sw}} \int_{t}^{t+t_{cond/D1b}+\Delta t_{off}} V_{D1b}(t) I_{D1b}(t) dt \\ &= V_{D1b}(t) I_{D1b}(t) D_D(t) dt \end{aligned} \tag{A17}$$

where $I_{D1b}\ (t)$ can be considered the fundamental output current and $V_{D1b}\ (t)$ is the on-state voltage drop across the diode. Several expressions can be determined as

$$I_{D1b}\ (t) \approx I_L(t) = I_M \sin(\omega_o t) \tag{A18}$$

$$V_{D1b}(t) = V_{t/D} + a_D I_{D1b}^{b_D} \tag{A19}$$

$$D_D\ (t) = \frac{1}{2}[1 - M\sin(\omega_o t + \varphi_o)] \tag{A20}$$

$$E_{off\ /D1b}(t) = 0.5 I_{rr}\ 0.5 V_{dc} t_b \tag{A21}$$

The average conduction power losses can be expressed after substituting (A18)–(A20) in (A17) as

$$P_{cond/D1b}\ (t) \approx I_M \sin(\omega_o t)\left[V_{t/D} + a_D I_{D1b}^{b_D}\right] 0.5[1 - M\sin(\omega_o t + \varphi_o\ )] \tag{A22}$$

Meanwhile, switching losses of diode (D1b) can be expressed as below:

$$P_{\frac{off}{D1b}}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{cond/D1b}}^{t+t_{cond/D1b}+\Delta t_{off}} V_{D1b}(t) I_{D1b}(t) dt = \frac{E_{off/D1b}(t)}{T_{sw}} \tag{A23}$$

Total power losses of diode (D1b) can be expressed as below

$$P_{D1b}(t) \approx\ V_{D1b}(t) I_{D1b}(t) D_D(t) + \frac{E_{off/D1b}(t)}{T_{sw}} \tag{A24}$$

Substituting (A18)–(A21) in (A24), then

$$P_{D1b}(t) = \left(V_{t/D} + a_D I_{D1b}^{b_D}\right)(I_M \sin(\omega_o t))\left(\frac{1}{2}[1 - M\sin(\omega_o t + \varphi_o)]\right) + \left(\frac{0.5 I_{rr}\ 0.5 V_{dc} t_b}{T_{sw}}\right) \tag{A25}$$

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