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SPICE Simulation Assisted-Dynamic $R_{DS(ON)}$ Characterization in 200V Commercial Schottky p-GaN HEMTs Under Unstable Phases

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Abstract. This paper presents a comprehensive analysis of dynamic and static $R_{DS(ON)}$ in Schottky p-GaN High Electron Mobility Transistors (HEMTs), highlighting the impact of off-state and hot electron trapping on device performance. The authors observed significant hysteresis in the transfer characteristics of a 200V commercial Schottky p-GaN, attributing this to charge trapping effects. A novel experimental setup, employing a multi-pulse test synchronous buck converter circuit with additional gate control and a clamping circuit, enabled precise characterization of dynamic $R_{DS(ON)}$ under varying conditions, including unstable phases with overcurrent. This method effectively mimics solar PV input scenarios, exposing the device to high dv/dt and di/dt stresses, which are critical for evaluating GaN device stability under transient conditions. This research also reveals that increased gate resistance reduces energy losses, challenging traditional expectations by demonstrating the nuanced gate charge dynamics of GaN HEMTs. This study overall contributes to the understanding of GaN device behavior, offering a novel approach for accurately characterizing dynamic $R_{DS(ON)}$ under unstable stages, furtherly advances the GaN device in complex renewable energy power converter applications.

1. Introduction

In the evolving landscape of power semiconductor devices, Schottky p-GaN High Electron Mobility Transistors (HEMTs) have emerged as a competitive candidate, particularly due to their exceptional efficiency and performance in medium voltage applications [1], [2]. The surge in their popularity is primarily attributed to their potential in revolutionizing power converter applications through size reduction and enhanced energy efficiency [3]. While existing literature extensively explored Schottky p-GaN in both device and circuit level, the dynamic behavior of dynamic on-resistance ($R_{DS(ON)}$) under unstable transient conditions, an area crucial for the reliable operation of power electronics, remains underexplored [4], [5], [6]. This problem becomes especially pronounced in scenarios that under solar photovoltaic (PV) inputs, where the devices are subjected to extreme dv/dt and di/dt stresses and overcurrent, making the understanding of their behavior under these conditions imperative for their application in renewable energy systems [7], [8].

This research aims to bridge the gap by developing a novel multi-pulse test synchronous buck converter circuit. This design facilitates the precise characterization of dynamic $R_{DS(ON)}$ in Schottky p-GaN HEMTs under both stable and unstable conditions. This approach enables the devices' behaviors under transient states and time-variable step inputs, closely simulating the solar PV scenario where input voltage fluctuates with instantaneous solar irradiance changes. Utilizing LTSpice simulations, the proposed methodology has been validated to effectively characterize the dynamic resistance across various conditions. Furthermore, this research examined the impact of gate on-resistance ($R_{GS(ON)}$) on gate and drain voltage waveforms, alongside the characterization of Device Under Test (DUT) conduction losses as influenced by variations in $R_{GS(ON)}$ and input voltage stress. The data obtained from LTSpice simulations reveal that energy losses in the DUT decrease with an increase in $R_{GS(ON)}$ for a 200V commercial P-GaN HEMT device.

The paper is organized in a systematic and detailed manner. Section II delves into the structural complexities and mechanisms of hot electron and off-state trapping in Schottky p-GaN HEMTs. Section III introduces the proposed multi-pulse test (MPT) circuit and discusses the unstable stage of the testing circuit characterized by overcurrent, peak overshoot, and damping oscillations, observed under LTSpice simulations within the proposed scenario. Section IV elaborates on the simulation design for characterizing dynamic $R_{DS(ON)}$ during both the initial unstable and subsequent stable phases, accompanied by corresponding data results. Section V explores the influence of the gate resistor on the DUT's gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}), particularly focusing on the waveform's rising time. Simulations of the three-cycle energy losses of the DUT, with input voltage and $R_{GS(ON)}$ as independent variables, are presented, providing insights into how increased gate resistance affects energy losses and device stability. Lastly, Section VI concludes the paper by summarizing the key findings and discussing the broader implications of this research in advancing the application of GaN HEMTs in renewable energy power converters, signifying a notable advancement in the field of power electronics.

2. Static Characteristics with Charge Trapping

2.1. Schottky P-GaN HEMT with Charge Trapping

Fig.1 illustrates a typical Schottky p-GaN HEMT structure, which leverages the high electron mobility of GaN and a metal-semiconductor (Schottky) junction for rapid switching, low on-resistance, and a normally-off state [3]. The device comprises a supporting substrate, a buffer layer to mitigate defects, an n-doped active GaN layer, and an AlGaN layer that forms a two-dimensional electron gas (2DEG) channel, essential for high electron mobility [9]. A metal layer creates the Schottky barrier with the AlGaN layer. Source and drain contacts are established with the 2DEG channel, with the source contact being ohmic to allow free charge carrier flow, and the drain contact forming the Schottky junction. The gate electrode, positioned directly on the AlGaN layer between source and drain, regulates the 2DEG channel's conductivity, making the device a voltage-controlled power switch. The operation of a Schottky p-GaN HEMT centers on modulating the 2DEG channel's conductivity at the AlGaN/GaN interface by applying a positive gate voltage, thus facilitating electron flow from source to drain. The Schottky barrier minimizes off-state leakage current and enhances switching speed [10].

Despite the 2DEG's superior semiconducting properties, charge trapping issues such as hot electron trapping during the turn-on phase and off-state trapping under high drain-source voltage stress can destabilize the device [11]. Hot electron trapping involves the entrapment of negative charges from the 2DEG into the dielectric and GaN layers, potentially leading to device failure. Off-state trapping, affecting electrons in buffer and GaN layers, complicates $R_{DS(ON)}$ characterization due to the variability of trapping effects. This necessitates precise $R_{DS(ON)}$ characterization to account for the complexities introduced by charge trapping, as highlighted in Figure 1.

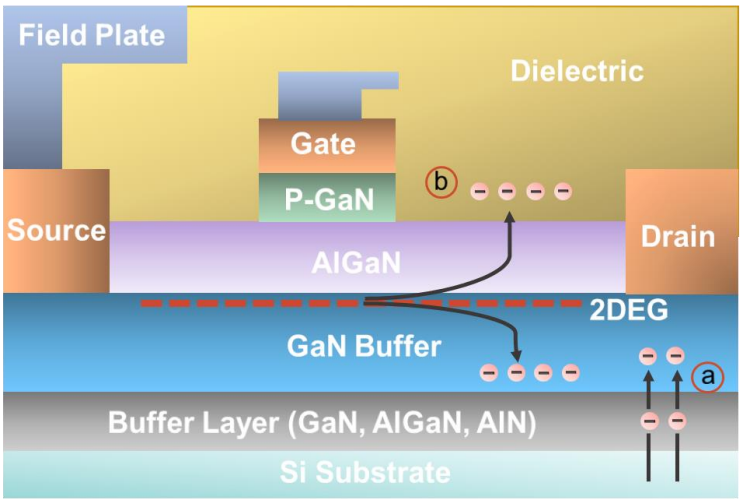

Figure 1. Cross section view of a Schottky p-GaN HEMT with charge trapping demonstration. (a) phenomenon of off-state trapping with locations. (b) hot-electron trapping with electron locations.

2.2. Trapping Validation by Device Static Characterization

To substantiate the charge trapping phenomenon, we investigated the static characteristics of a typical 200V commercial Schottky p-GaN using a Keysight B1505A Power Device Analyzer and an MPI TS200SE Probe Station, with the DUT probe connection shown in Figure 2. The data presented in Figure 3 delineated the transfer characteristics under a 100mA compliance with an SMU module. A forward and reverse voltage swept from 0 to 2.4V and back to 0V, exceeding the threshold voltage of the device, revealed a pronounced hysteresis, rather than the expected overlapping curves, thereby confirming the presence of charge trapping.

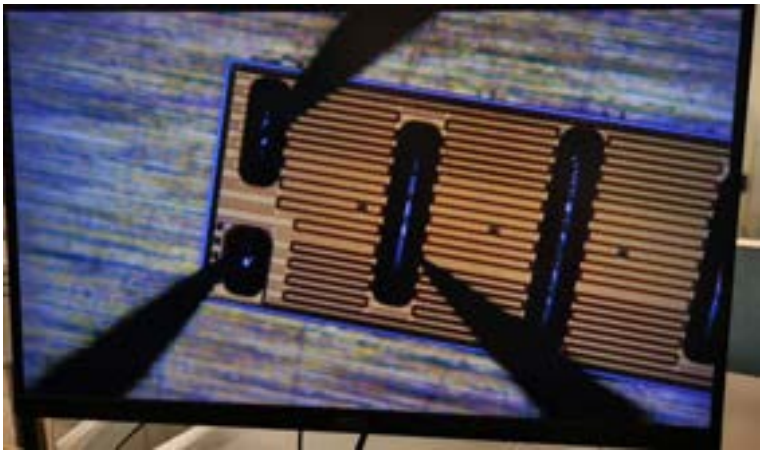

Figure 2. 200V commercial Schottky P-GaN static characteristic using Keysight B1505A Power Device Analyzer and MPI TS200SE Probe station.

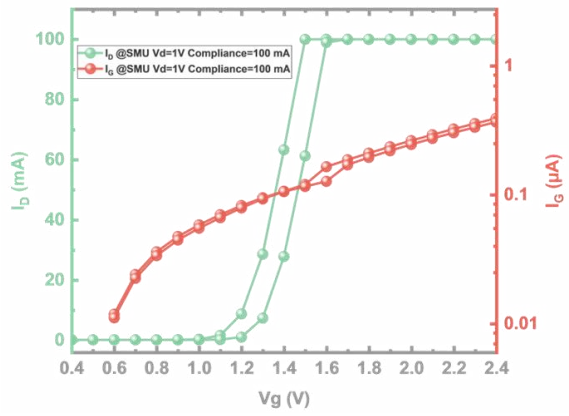

Figure 3. Initial transfer characteristics under a 100mA compliance.

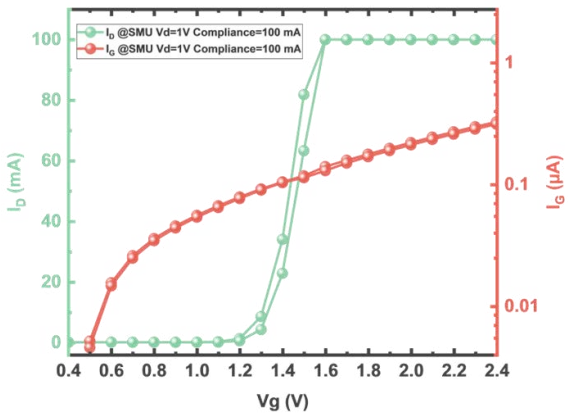

Figure 4. Transfer characteristics after 5 mins.

Subsequent repetitions of the test, illustrated in Figure 4, demonstrated a reduction in hysteresis, attributed to the accumulation of previously trapped charges. Moreover, the inherently low on-resistance of the 200V commercial p-GaN, which is significantly less than the parasitic resistance of the probe, rendered the measurement of static $R_{DS(ON)}$ challenging. To overcome this limitation, static SPICE simulations shown in Figure 5 were employed to estimate static $R_{DS(ON)}$ across various V_{DS} and temperature conditions, with an estimated variation from 6 mΩ to 17.7 mΩ when the gate is normally-on at +6V.

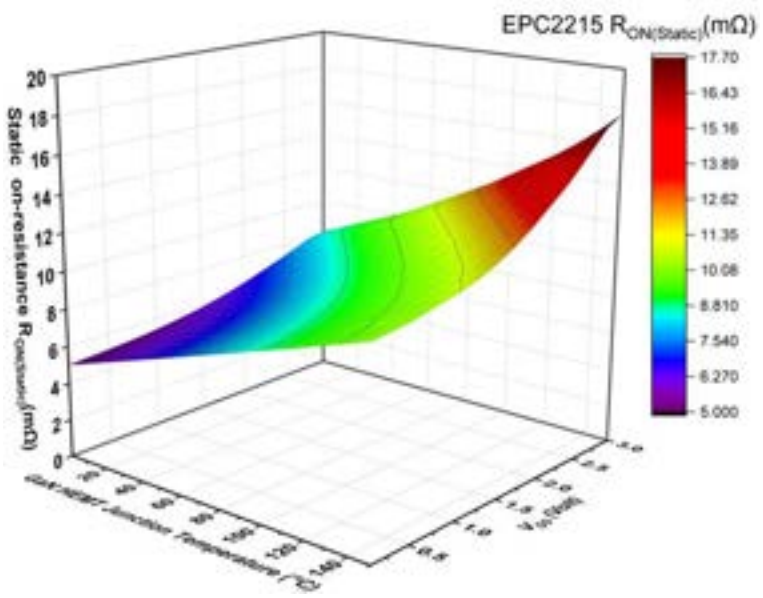

Figure 5. 200V commercial Schottky P-GaN static $R_{DS(ON)}$ SPICE simulation.

3. Testing Circuit Design under Unstable Stages

3.1. State-of-The Art of the Proposed Multi-Pulse Hard-Switching Circuit

To address the gap for commercial Schottky P-GaN HEMT circuit-level parameter characterization during unstable phases within DC-DC power converter applications, this study focuses on assessing the dynamic on-resistance under such conditions. Figure 6 presents an innovative circuit design aimed at this purpose. The design features a dual gate driver configuration controlling two GaN HEMT switches arranged in a half-bridge topology. This setup, combined with a supporting bulk inductor and capacitor,

forms a synchronous buck converter that enhances output waveform quality. Each transistor is paired with a dedicated gate driver, allowing for precise control over their switching moments. The use of a bootstrap circuit facilitates the management of high side switching, accommodating complex control algorithms. This approach deviates from traditional double pulse test (DPT) or multi-pulse test (MPT) setups, which typically focus on single switch pulse transition characteristics and lack the capability to thoroughly explore transient dynamics or support extended operational testing. The proposed configuration enables detailed measurement and protection during transients, offering an enhanced ability to evaluate the DUT across a wider range of operating conditions, outperforming existing DPT/MPT techniques [12]. A key innovation of this design is the incorporation of an extra gate digital signal control to precisely record the $R_{DS(ON)}$ initial switching time to enable the PWM pulse generator pre-configuration, alongside a novel clamping circuit designed to accurately characterize dynamic $R_{DS(ON)}$ in both unstable and stable states with the expression:

$$R_{DS(ON)} = \frac{V_m - \left[a \cdot \left(\frac{V_1 - V_m}{R_1} - \frac{V_m}{R_2}\right) + b\right]}{I_{D(DUT)}} \quad (1)$$

V_1 denotes the external voltage supply, whereas a and b symbolize the slope and intercept, respectively, of the high breakdown voltage SiC Diode's linear fit at ambient temperature. Additionally, the DUT drain current, $I_{D(DUT)}$, is determined using a coaxial shunt [13].

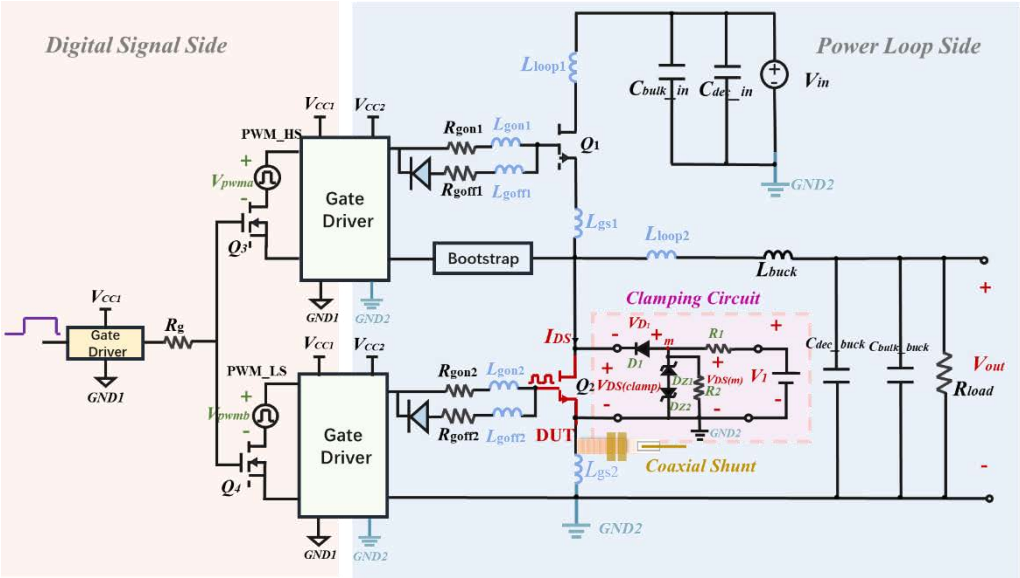

Figure 6. Proposed synchronous buck MPT converter with extra gate digital signal control and back-to-back clamping circuit design.

3.2. Testing Condition During Unstable Stages

To assess the behavior of testing circuit waveforms under unstable conditions, the experimental setup was designed that simulates a dynamic power input. This setup employs a time-variable step input to emulate the conditions found in solar PV systems, where the input voltage fluctuates in response to changes in instantaneous solar irradiance. The literature review indicates that such step inputs are commonly used to evaluate the performance of Maximum Power Point Tracking (MPPT) algorithms—including Perturb & Observe (P&O), Incremental Conductance (INC), and Global MPPT (GMPPT)—which are essential for advancing research into GaN power converters in PV applications [8].

As demonstrated in Figure 7, the simulation subjects the P-GaN switch to a rigorous test: the input voltage stress steps from 150V to 200V, drops to 100V, and then returns to 150V. Throughout these transitions, particularly during the 150V to 200V and 200V to 100V intervals, the P-GaN switch experiences significant dv/dt and di/dt stresses. These stresses are attributed to the rapid switching

capabilities of the E-GaN HEMT and the variability of the input voltage. Consequently, this leads to peak overshoots, undershoots, and oscillations, culminating in prolonged overcurrent conditions (lasting hundreds of microseconds), as shown in Figure 8. Such phenomena pose a considerable risk to the stability and longevity of GaN devices, potentially leading to device failure [14].

Figure 7. Unstable voltage output corresponding to stepping input voltage using LTSpice piecewise linear functions.

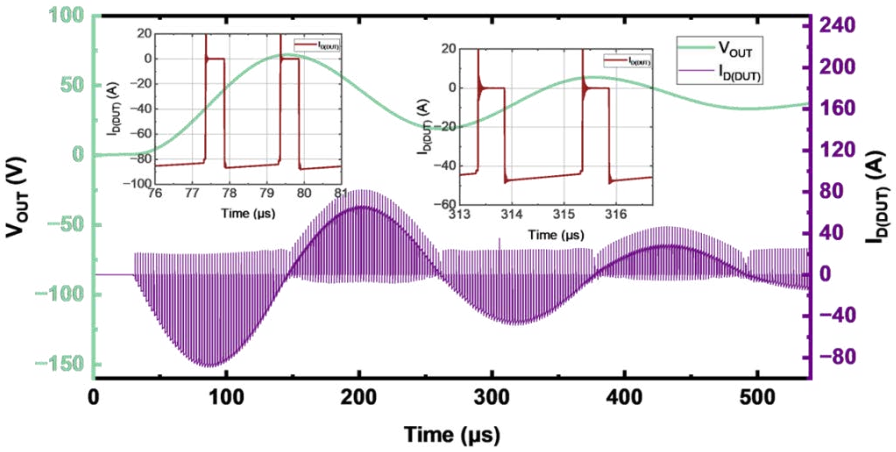

Figure 8. Output current and voltage waveform of the DUT within the initial unstable phase with overcurrent observation.

4. Simulation Setup and $R_{DS(ON)}$ Characteristics

As depicted in Table 1, the selection of components and the configuration of the simulation were conducted using LTSpice to facilitate the characterization of dynamic $R_{DS(ON)}$ under conditions of instability. The simulation outcomes are illustrated in Figure 9 and Figure 10. Given the unstable voltage output stage shown in Figure 7, particularly the phase with the highest peak overshoot and overcurrent, the 150V-V_{IN} stage was chosen for detailed analysis. This selection was aimed at characterizing the initial unstable period effectively. The simulation examined the dynamic $R_{DS(ON)}$ at two key intervals: the initial onset of instability (38µs) shown in Figure 9, and during a subsequent stable transient state (652µs) at Figure 10. The results revealed an initial dynamic $R_{DS(ON)}$ of 10.4 mΩ during the early unstable phase, which then increased to approximately 13.1 mΩ in the stable phase. These findings indicate a 30% increase in dynamic $R_{DS(ON)}$ compared to the static $R_{DS(ON)}$ during the initial phase of instability. Furthermore, a 64% increase in dynamic $R_{DS(ON)}$ was observed during the stable conduction phase after 650µs. It is imperative to acknowledge that the fidelity of the simulation results extends to the granularity of the clamping circuit and the commercial P-GaN HEMT equivalent subcircuit model. However, these simulations do not encapsulate accumulated charge trapping phenomena and other nuanced device-level

behaviors. Consequently, there may be discrepancies between our simulated outcomes and those observed in empirical scenarios. This limitation underscores the need for cautious interpretation of the simulation data, as the exclusion of such intricate device-level dynamics might lead to variations from actual experimental results [15].

Table 1. LTSpice Testing Circuit Parts Selection and Transient Simulation Setup.

PWM Signal Control	**Half-Bridge Power Loop**	**Clamping Circuit for $R_{DS(ON)}$ Testing**
signal control gate driver: LTC7001 Half bridge gate driver: ADUM4121A Control signal MOSFET switch: Si7234DP	P-GaN HEMT DUT: EPC2215 Bootstrap Diode: C3D1P7060Q $R_{G(OFF)}$ blocking diode: 1N5817	Voltage divider resistor: R=200 Ω Blocking Diode: C3D02065E Zener Diode: UM25-1N
Simulation Transient Setup		
PWM control: $V_{initial}$=0 V; V_{ON}=9 V; T_{delay}=30μs; T_{rise}=20ns; T_{fall}=20ns; T_{ON}=1ms; T_{period}=1ms PWM_1: $V_{initial}$=6 V; V_{ON}=0 V; T_{delay}=0 s; T_{rise}=20 ns; T_{fall}=20 ns; T_{ON}=1.483μs; T_{period}=2μs PWM_2: $V_{initial}$=0 V; V_{ON}=6 V; T_{delay}=50 s; T_{rise}=20 ns; T_{fall}=20 ns; T_{ON}=1.383μs; T_{period}=2μs V_{CC1}=9 V; V_{CC}=5 V; V_{DD}=5.5 V; V_1=10 V; R_{load}=60 Ω; L_{buck}=20μH; C_{buck}=90μF; C_{IN}=47μF; V_{IN}=PWL(150,200,100,150) V		

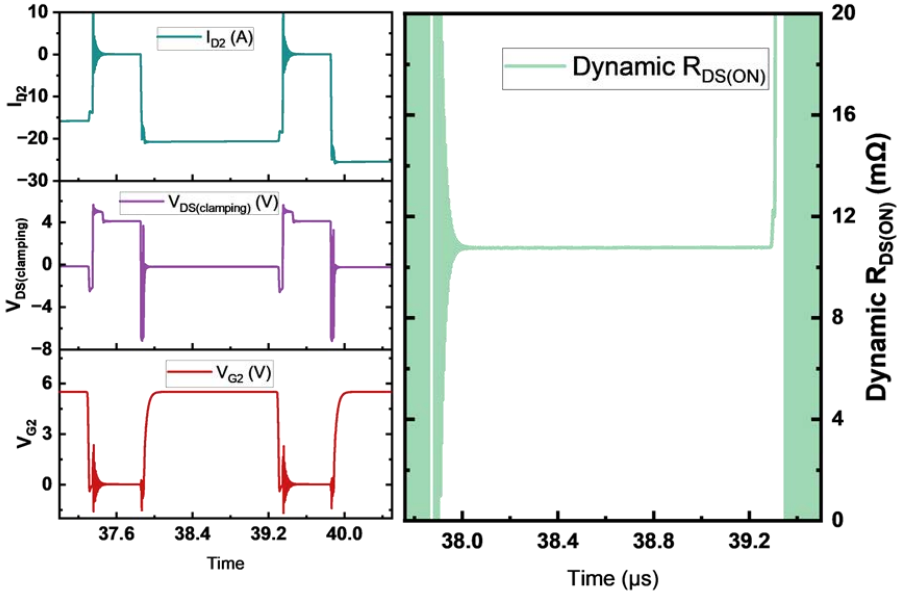

Figure 9. Simulated Dynamic $R_{DS(ON)}$ during initial unstable switching transient.

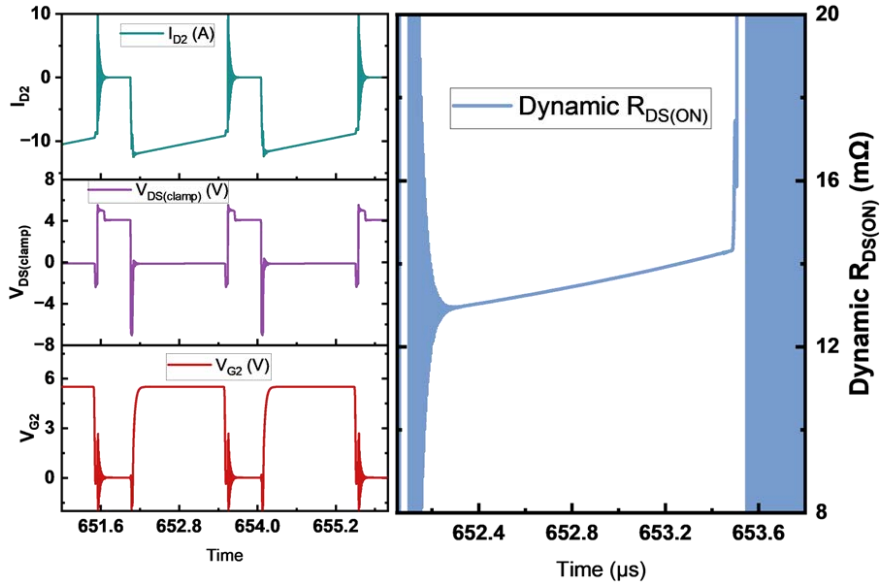

Figure 10. Simulated Dynamic $R_{DS(ON)}$ during stable switching transient.

5. Influence of Gate Resistance on Energy Losses

Furthermore, the impact of $R_{G(ON)}$ on V_{GS} and V_{DS}, revealing its influence on the switching duration of V_{DS} and the rise time of the gate pulse, were investigated as detailed in Figure 11 and Figure 12. An increase in $R_{GS(ON)}$ notably extends the rise time of the V_{GS}, leading to a longer turn-on period without substantially affecting the turn-off timing. Additionally, variations in $R_{GS(ON)}$ impact the transients of V_{DS} across both switching phases, indicating a correlation between switching speed and gate resistance levels. Particularly, excessively low $R_{GS(ON)}$ values induce ringing oscillations.

This behavior can be traced back to several foundational mechanisms identified in our previous research [16]. Firstly, a diminished gate resistance facilitates swift charging and discharging of the gate's capacitance, accelerating the turn-on and turn-off processes. While such rapid switching is generally advantageous, it can lead to undesirable outcomes, including voltage overshoots and ringing in V_{GS} and V_{DS}, driven by heightened di/dt and dv/dt rates that excite the circuit's parasitic inductances and capacitances, resulting in oscillatory behavior. Furthermore, the Miller effect, which amplifies the capacitance between the gate and drain (C_{GD}) during swift dv/dt transitions, compounds these challenges [17]. This effect slows the switching speed momentarily due to a significant voltage variation across C_{GD}, leading to dynamic feedback that may cause additional voltage overshoots and ringing. The presence of low gate resistance exacerbates this effect by diminishing the gate drive circuit's control over the gate's charging and discharging, thereby increasing the circuit's susceptibility to feedback oscillations. In addition, the high-speed switching nature of GaN HEMT circuits inherently amplifies sensitivity to layout parasitic, including inductances and capacitances. These parasitic elements, when resonating with the rapid switching transitions, can induce ringing. The frequency of such oscillations typically correlates with the LC resonance frequency, incorporating parasitic inductances from the package leads, printed circuit board (PCB) traces, and connections, as well as the device's inherent capacitances and any additional external capacitance. In this simulation study, external parasitic inductances were accounted in the testing circuit.

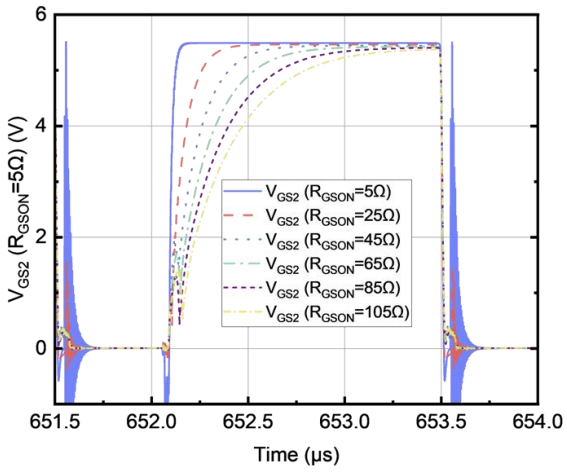

Figure 11. $R_{GS(ON)}$ influence on V_{GS} rising time.

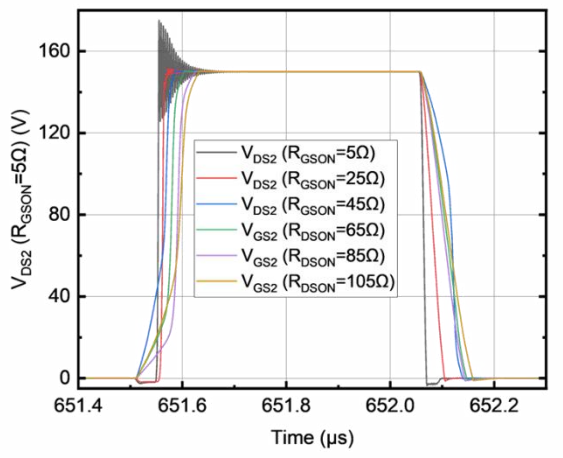

Figure 12. $R_{GS(ON)}$ influence on V_{DS} switching speed.

Further simulations aimed at quantifying energy losses in the DUT across varied input voltages and $R_{GS(ON)}$ values from 2 ohms to 45 ohms demonstrate a direct correlation between energy losses and input voltage, and an inverse correlation with increasing $R_{GS(ON)}$, as shown in Figure 13. This finding challenges the traditional expectation that higher gate resistance leads to increased switching losses due to reduced switching speeds [18]. The simulations reveal that, for a 200V commercial P-GaN HEMT, increasing $R_{GS(ON)}$ decreases energy losses.

This deviation can be attributed to the unique gate charge dynamics of GaN HEMTs, where a low $R_{G(ON)}$ may cause voltage overshoots during rapid charging and discharging, increasing losses. Moreover, a higher $R_{GS(ON)}$ moderates switching transitions, effectively reducing losses by minimizing excessive overshoot and ringing. This observation is supported by the noted increase in peak drain currents (I_D) with lower $R_{GS(ON)}$, explained by the quicker charging and discharging of the gate due to a lower RC time constant, leading to faster transistor turn-on and a consequent rise in I_D. Additionally, the overshoot of gate voltage beyond the threshold for a longer duration with lower $R_{G(ON)}$ facilitates more robust channel current flow, further elevating I_D peaks. These insights underscore the intricate interrelation between gate resistance and device performance, challenging established paradigms and suggesting avenues for further exploration in GaN HEMT applications.

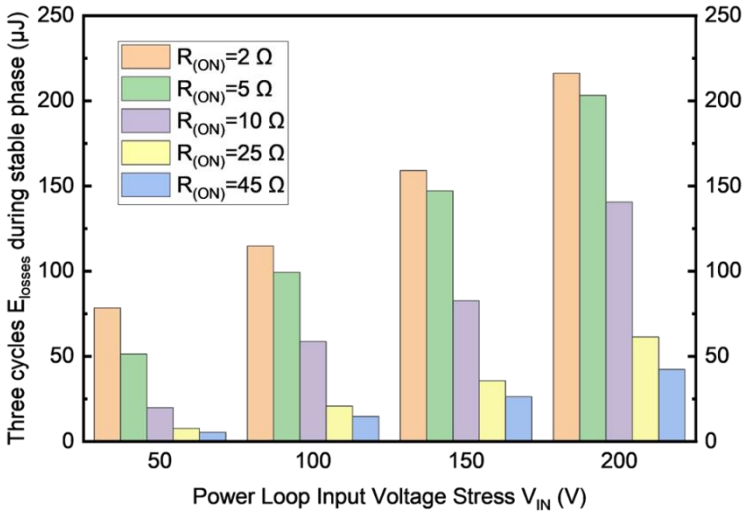

Figure 13. Energy losses within three cycles (6μs) of the stable state with respect to V_{IN} and $R_{G(ON)}$.

6. Conclusion

This study addresses the underexplored dynamics of dynamic $R_{DS(ON)}$ in Schottky p-GaN HEMTs under transient conditions, crucial for their deployment in solar PV applications. By developing a novel multi-pulse test synchronous buck converter circuit, together with LTSpice simulations, $R_{DS(ON)}$ was precisely characterized across both stable and unstable states, closely mimicking real-world solar PV MPPT voltage input scenarios. This research reveals that $R_{GS(ON)}$ significantly influences device performance, notably demonstrating that increased $R_{GS(ON)}$ reduces energy losses in a 200V commercial P-GaN HEMT. This counters traditional expectations by suggesting that higher $R_{GS(ON)}$ can actually improve device stability and efficiency by mitigating rapid gate charging and discharging, minimizing ringing oscillations exacerbated by the Miller effect and circuit parasitic. These insights effectively fill a critical knowledge gap regarding the behavior of Schottky p-GaN HEMTs under varying electrical stresses and lay a foundation for further advancements in power electronics, enhancing the efficiency and reliability of GaN HEMT-based power converters in renewable energy applications.

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