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Low Quiescent Current 110 nm Capacitorless Low Dropout Voltage Regulator with Wide Load Current Range

Wan Maziyah Ab. Halim[1], Julie Roslita Rusli[1]*, Yuzman Yusoff[2], Suhaidi Shafie[3], Suraya Shaban[4]

[1] *Universiti Kuala Lumpur British Malaysia Institute, Batu 8, Jalan Sungai Pusu, Gombak, 53100, MALAYSIA*
[2] *Symmid Corporation Sdn. Bhd, Plaza Sentral, Jalan Stesen Sentral 5, KL Sentral, Kuala Lumpur, 50470, MALAYSIA*
[3] *Faculty of Engineering, Universiti Putra Malaysia, 43400, MALAYSIA*
[4] *The University of Electro-Communications, Tokyo, JAPAN*

*Corresponding Author: julie@unikl.edu.my
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Capacitorless LDO, LDO, CLDO, wide range, quiescent, capacitorless, load range

Abstract

Recent developments in Internet of Things (IoT), sensor-based mobile devices, implantable devices and smart wearables have fueled the demand for power-efficient and compact system-on-chip (SoC) solutions, causing power management in integrated circuit (IC) designs to become crucial. As low dropout (LDO) voltage regulators have become one of the key components in power management systems, capacitorless LDO (CLDO) voltage regulators are also becoming more popular due to their compactness which offers better power and cost-effectiveness compared to conventional LDO regulators. Power durability has become critical because longer battery life is highly preferred in portable devices, and this highlights the importance of minimizing the power consumption of the devices so that the battery discharges at a slower rate. An effective way to reduce the power in a CLDO regulator is to keep its current flow during idle mode, which is called the quiescent current, at a minimum level. This paper presents a low quiescent current CLDO regulator operating at a nominal voltage of 1.2 V with a regulated output voltage of 1 V utilizing the 110 nm CMOS technology. The proposed CLDO regulator achieved a low quiescent current of 5.18 µA with a wide range of load current up of 200 mA at maximum and 80% improved line regulation from the previous work with the same voltage requirements. The single-digit micro-ranged quiescent current greatly contributes in minimizing power consumption during the idle mode of the CLDO regulator which can be within single digit micro-Watt range where ultra-low power applications operate, thus prolonging the battery life, whilst the wide load range provides flexibility for the proposed CLDO regulator to power a larger range of circuits to drive with better line regulation and relatively good PSRR at low-frequency range.

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1. Introduction

Complementary metal-oxide semiconductor (CMOS) technology and integrated circuit (IC) design has developed to the point where electronic appliances are made compact, stand-alone and power-savvy. Recent developments in Internet of Things (IoT), sensor-based mobile devices, implantable and smart wearables have also fueled the demand for power-efficient and compact system-on-chip (SoC) solutions, causing power management in IC designs to become a critical key factor [1], [2]. A system may consist of multiple blocks with different functions that vary from supplying voltage, reading external parameters, converting data, to performing calculations, etc. These multiple sub-blocks might have different voltage requirements. The input voltage powering the system might come from different sources with voltage variations and might not be sufficient to supply all the different operating voltage requirements for each block. Therefore, each system will have its own power management structure to manage its internal voltage supplies. In low-power IC design, especially noise-sensitive circuits such as sensor-based circuits which are widely used in IoT systems, it is crucial to provide a clean and stable input voltage to the sub-blocks with minimal noise to ensure accuracy and good performance. This can be achieved by the utilization of an LDO voltage regulator which regulates an output voltage from a fixed input voltage in a simple and inexpensive way to supply the required voltage by the circuits it drives, resembling an ideal voltage source in real-life implementation [3], [4]. As an example, an IoT-enabled building energy management system that harvests the electricity from a solar panel will need to store the energy before it can be reused to power the sensors and the smart switches in the system as illustrated in Fig. 1. A power management block in which the LDO regulator is one of the key components is crucial in a system that utilizes energy harvesting units sensor-based devices such as the IoT-enabled building system because the stored energy has to be processed and managed so that all stringent voltage requirements coming from the different parts of the IoT system can be fulfilled and the signals coming from the sensors can be accurately converted and processed.

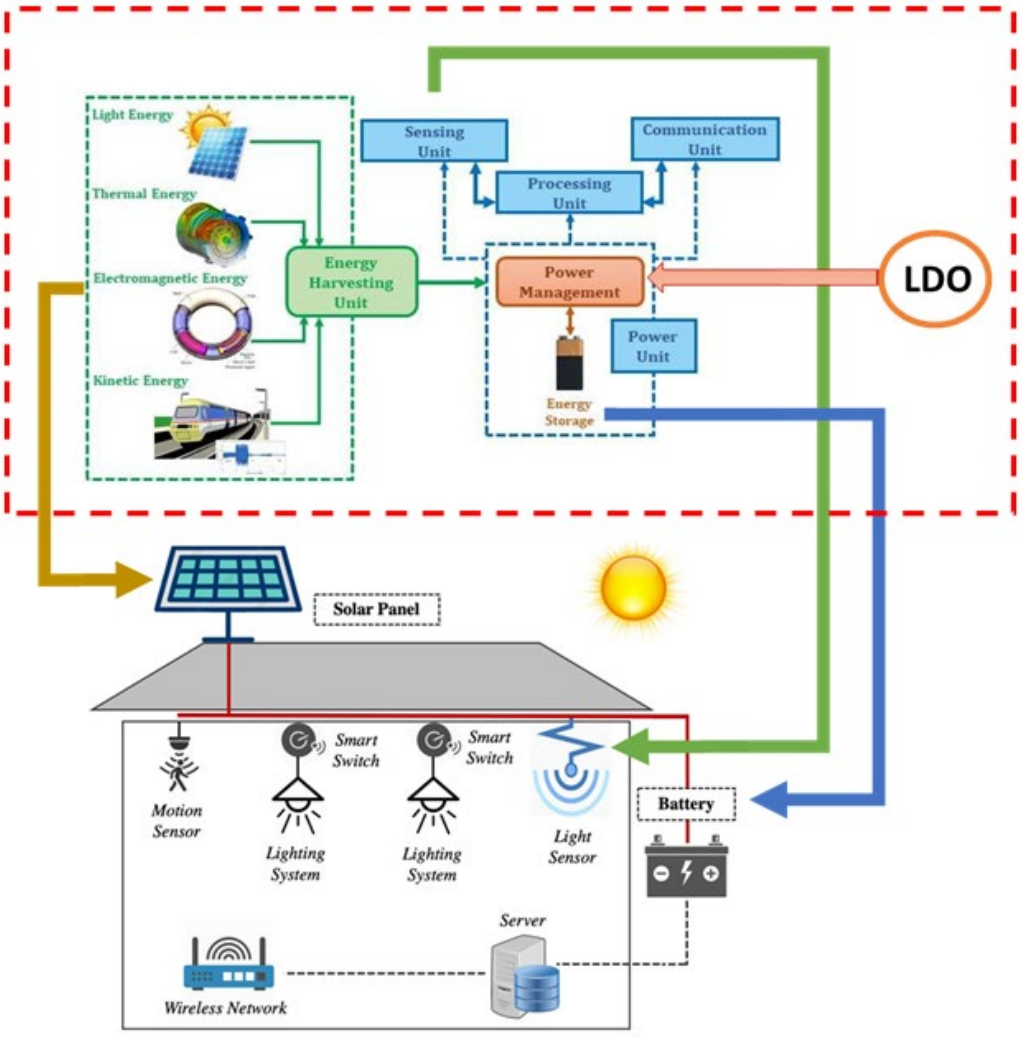

Fig. 1 *LDO regulator in power management of an IoT-enabled building energy management system [5], [6]*

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As one of the widely used power management circuits, the demand for low-power LDO voltage regulators is greatly increasing, and the ability to make it compact in a complete SoC design while maintaining required key performance criteria is highly anticipated so that the printed circuit board (PCB) area can be reduced thus reducing its power and manufacturing cost. However, the large external output capacitor of a conventional LDO regulator has become the prohibiting factor in achieving this. A conventional LDO regulator operates with a bulky external output capacitor to maintain its stability and good performance. Based on Fig. 2, this bulky output capacitor C_L has a very large capacitance value and can only be realized in the form of an external circuit element, preventing the LDO regulator from being able to be fully on a chip. Extra areas are required to place the input-output (I/O) pads for the external connections which also means extra pins are needed for the same purpose. Due to this factor, 'capacitorless' LDO (CLDO) regulator has come into frame to solve the external capacitor issue. A CLDO is achieved by removing the large external capacitor, and the implementation will reduce the number of I/O pads and pins, hence reducing the effective area of printed circuit board (PCB) which will also reduce the cost of manufacturing. The absence of a large output capacitor will also greatly reduce the power consumption of the CLDO regulator. This, however, does not suggest that the output capacitance is totally omitted, but on the other hand is reduced and compensated to a level where the capacitance value makes it possible to be built internally within the LDO regulator while maintaining the overall performance of the LDO.

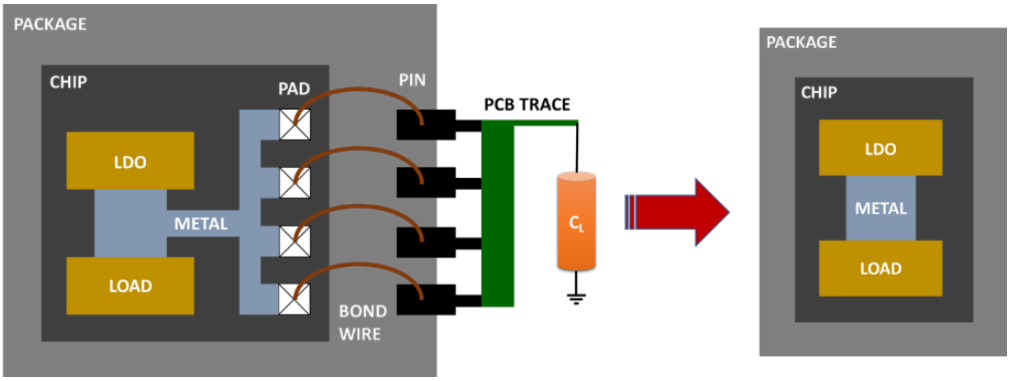

Fig. 2 *Comparison of a conventional LDO (left) vs capacitorless LDO (right) on a chip [7]*

A CLDO mainly consists of four main parts which are the error amplifier, the pass transistor, the feedback network and the load [8]. The only difference it has from conventional LDO regulator topology is the position and the size of the load capacitor C_L, whereas the C_L of the conventional LDO regulators is external and much bigger in size. At the same time, the C_L of a CLDO is built internally and much smaller in size, as depicted in Fig. 3. Even though the removal of the large external output capacitor in the CLDO regulator brings the mentioned advantages, it also introduces a drawback of degraded stability of the CLDO since the large output capacitor greatly contributes to the stability and noise rejection which are crucial for a good LDO regulator [9]. Multiple circuit techniques have been proposed throughout the years to overcome the disadvantage of operating without the large external capacitor and to enhance the performance of CLDO regulators in several key areas such as advanced compensation techniques to improve stability of the CLDO regulator [10]–[12], load transient improvement circuits to improve transient performance of the CLDO regulator [13]–[15] and power supply rejection (PSR) enhancement topologies to improve the power supply rejection ratio (PSRR) of the CLDO regulator [14]–[19]. However, as the current trend revolves mainly around ultra-low powered devices such as energy-harvested portable devices, sensor-based devices for IoT, smart wearables, medical implantable devices, etc., power durability has become critical because longer battery life is highly preferred in such devices to avoid them from being charged too frequently, or even worse, to be replaced in a short time such as in the case of implantable medical devices, which involves operations on the human body. This highlights the importance of minimizing the power consumption of the devices to prolong the battery life and reduce charging frequency.

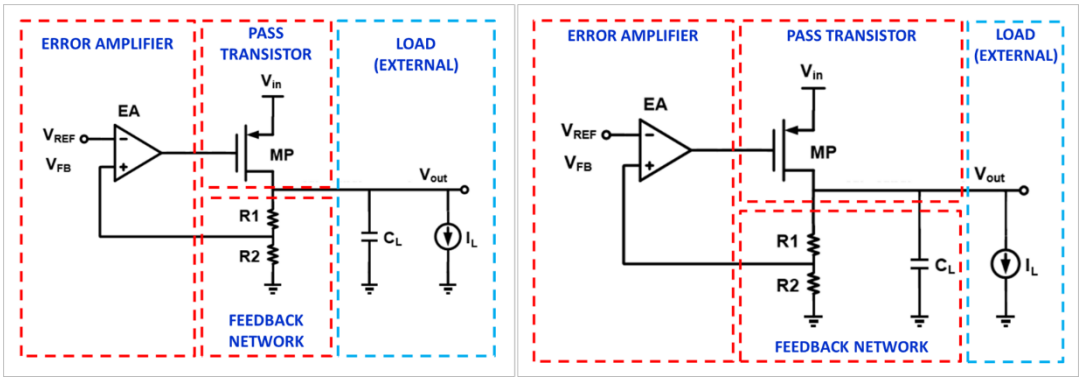

Fig. 3 *Basic topology of (a) conventional LDO; and (b) CLDO*

Technically, power depends on the current and voltage of a circuit. Therefore, the power consumption of CLDO regulators can be reduced either by lowering the voltage supply of the system or minimizing the current. Since a CLDO regulator functions when it is regulating a certain load current and is idle when there is no load current, an effective way to save power is to keep its current during idle mode at a minimum level. This current during idle mode is called quiescent current. It is the current when the CLDO has zero load and is depicted as the difference between input and output current [19]. If the quiescent current of the CLDO is relatively high, more power will be dissipated and the battery will be discharged faster. Therefore, it is crucial to obtain a very low quiescent current for the CLDO regulator in order to minimize its power dissipation during idle mode thus prolonging its battery life. This paper presents a low quiescent current CLDO regulator design with a wide load range operating at a nominal voltage of 1.2 V with a regulated output voltage of 1 V utilizing the 110 nm CMOS technology. The design approach and process are explained in the second section of the paper and the obtained results are discussed in the third section of the paper. The fourth section, which is the final section of the paper, concludes the work presented.

2. Proposed CLDO Design

The design process of the proposed CLDO regulator starts with defining the reference current as described in the flow chart in Fig. 4. Since this design utilizes a p-channel metal-oxide semiconductor (pMOS) input error amplifier, the current mirror used is also of a pMOS type. Referring to the schematic view in Fig. 5, pMOS Q1 is simulated to determine its size with a reference current that is kept at a minimum value sufficient for it to operate in a saturated region. This is important in achieving low quiescent current because the reference current will be the minimum benchmark current in the error amplifier and the other nodes will be the multiplication of the reference current either the same value or higher in magnitude. Achieving a low current error amplifier will contribute to reducing the quiescent current of the CLDO regulator. The process is then followed by the design of the error amplifier. Since this reference current will be mirrored by the tail current of the error amplifier, it is advantageous if the value of *vb* can be precalculated so that *va* is known in advance to ensure the correct voltage drop is obtained while designing Q1. This is because ideally, it is required for *vb* to be exactly similar to *va* to achieve an accurate current mirror with the voltage *vb* sufficient enough to cover the required voltage range for the error amplifier. Q2 is then sized according to the amount of current desired at the tail node by multiplying the width of Q1 with the calculated factor. The process is continued with the sizing of the pMOS input pair transistors Q3 and Q4 of the error amplifier. Proper sizing of the input pair transistors contributes to the gain performance of the error amplifier since the transconductance g_m of the input pair transistors is one of the factors that affect the obtained gain. It is also advisable to avoid using the minimum length for the input pair transistors to avoid mismatch issues which will affect the performance of the error amplifier. The active load transistors Q5 and Q6 are sized so that the output voltage of the first stage of the error amplifier *vd* is sufficient to drive the second stage n-channel metal-oxide semiconductor (nMOS) Q8. The current at the second stage node determines the size of the second stage current mirror pMOS Q7 and the second stage output voltage *vea* determines the size of Q8. In this case the output voltage *vea* should be able to drive the pass transistor Q9 of the CLDO regulator. The error amplifier is then simulated to obtain the initial performance results. Direct-current (DC) analysis is performed to ensure that all transistors Q1-Q7 are in saturation region to prevent change of amplifier characteristics due to changes in transistor region. The saturation region is denoted as 'region 2' in simulator used for the design. After the completion of the error amplifier design, the feedback network follows. The current at this node will also be the current of the pass transistor during zero load. To achieve a low quiescent current, the current at this node is also kept at a relatively low level. Since the CLDO regulator output voltage and reference voltage are defined, the

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resistance value of resistor R1 is calculated based on the current decided at the feedback network and the known output voltage. The same goes for R2 with the voltage being the feedback voltage instead of output voltage which is the same as the reference voltage. The effect of the physical dimension of the resistors on the performance is also considered while deciding the width, length, and number of fingers of the resistors. The proposed CLDO regulator utilizes the Miller compensation method with dual compensation paths, one for high load compensation and another for low load compensation. The next stage is to design the pass transistor of the CLDO regulator. This CLDO regulator utilizes pMOS as its pass transistor due to its source-follower configuration which provides better voltage regulation with simple biasing and better input noise rejection. The pass transistor is sized so that it is strong enough to drive the maximum load of the CLDO regulator, therefore its size is much larger compared to the other transistors in the CLDO regulator. The length, however, is kept at the minimum to allow fast transient of the CLDO regulator. The CLDO is then simulated and verified for its functionality and characterized for its overall performance before the enable circuit is added to it. This circuit will enable the CLDO regulator when an enable signal is passed and reset the CLDO when the signal is removed. This addition will not affect the overall performance of the CLDO regulator and can be added after all the needed verifications are completed.

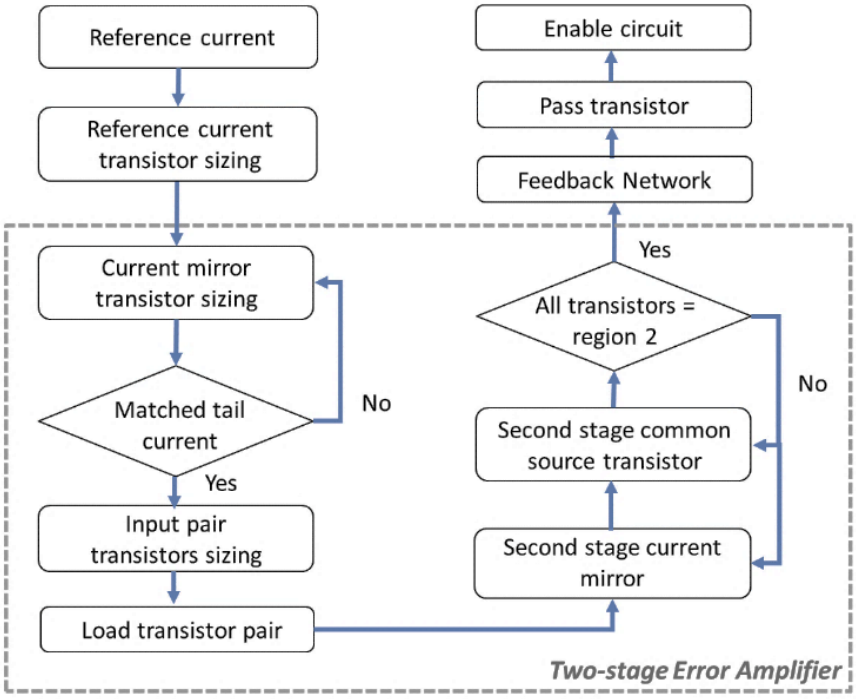

Fig. 4 *Flow chart of the proposed CLDO design*

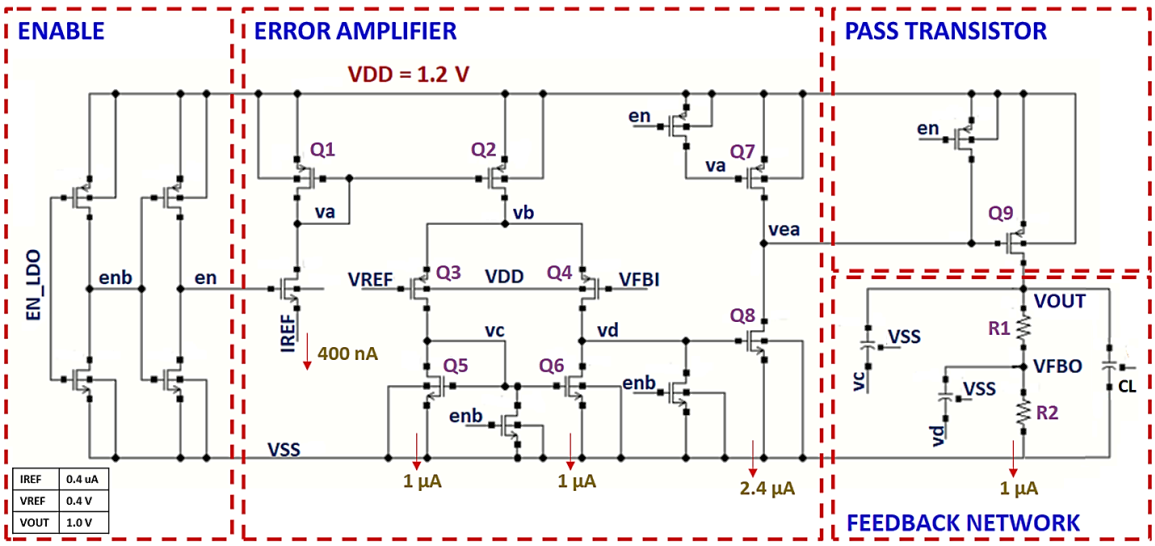

Fig. 5 *Full schematic of the proposed CLDO design*

3. Results and Analysis

The proposed CLDO regulator is simulated and verified, and the obtained results are discussed in this section. The overall verification of the CLDO regulator includes DC analysis for operating points, current and voltage verification, transient simulation for functional and timing results, and alternating-current (AC) analysis for frequency responses. DC analysis determines the drop-out voltage, load current range, line regulation and load regulation of the CLDO regulator while transient simulation verifies the functionality in terms of its ability to regulate the anticipated output voltage and provides timing information of the CLDO regulator. AC analysis is done to monitor the stability of the CLDO regulator and to obtain the gain, unity gain bandwidth, phase margin and the PSRR.

3.1 DC Analysis

Fig. 6(a) shows the DC sweep of the output voltage V_{OUT} across the input voltage V_{DD}. Based on the curve, V_{OUT} starts to regulate at the expected value of 1.0 V when V_{DD} is 1.1 V. This means the dropout voltage of the CLDO regulator is 0.1 V, which is the difference between 1.1 V and the output voltage of 1.0 V. From the load current I_L sweep curve in Fig. 6(b), it is shown that the CLDO regulator regulates the 1.0 V output voltage across the load current ranging from 0A up to 200 mA. The curve starts to degrade when the load current I_L goes beyond 220 mA. The line regulation of the proposed CLDO regulator is 56 µV/V, which shows an 80% improvement compared to prior work of similar voltage specs as shown in Fig. 7(a), while the load regulation is 110 µV/mA as shown in Fig. 7(b). Small line regulation means that the CLDO regulator can maintain the regulated voltage with minimum variation regardless of changes that occur in input voltage V_{DD}, which is a critical criterion of a CLDO regulator.

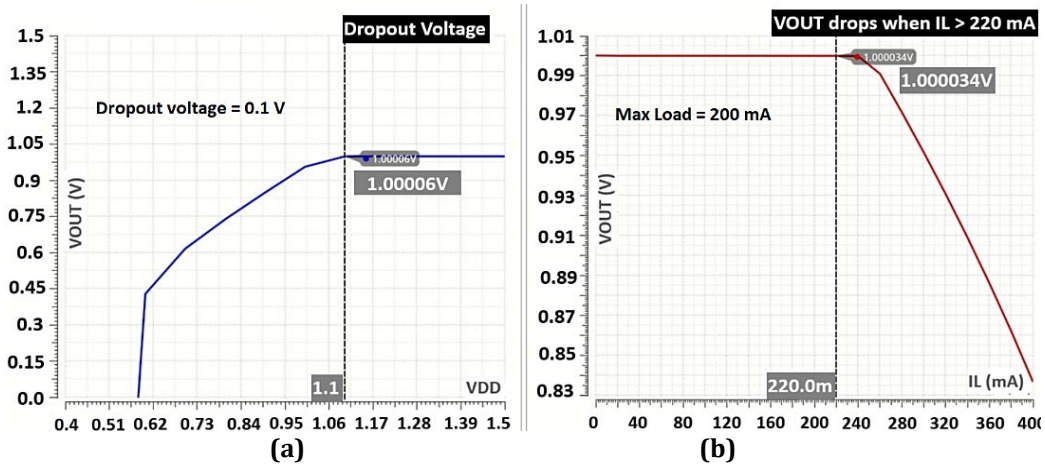

Fig. 6 *Dropout voltage (a) and maximum load current; (b) of the proposed CLDO regulator*

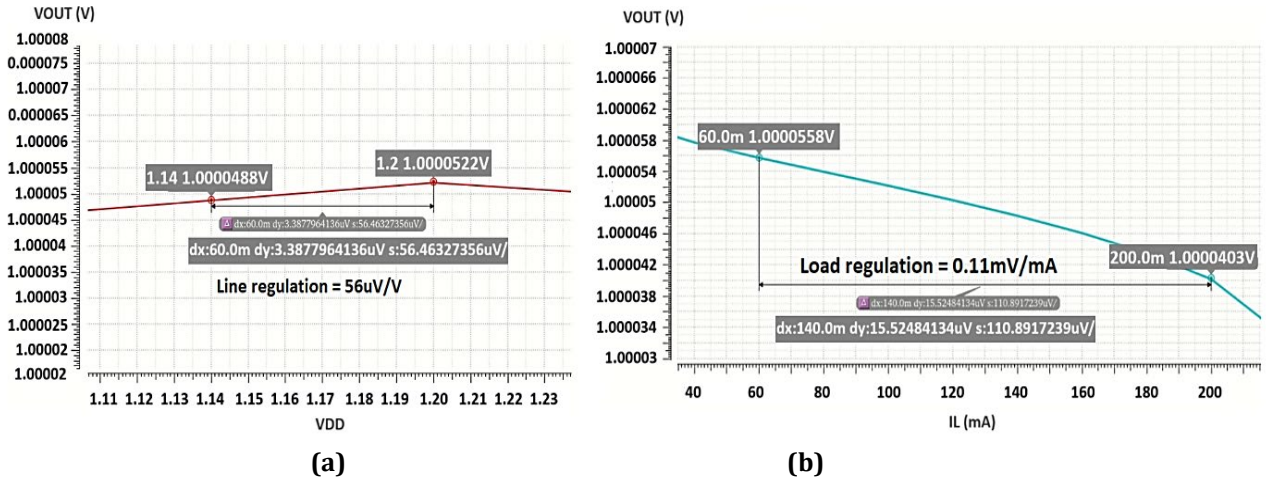

Fig. 7 *Line regulation (a) and load regulation; (b) of the proposed CLDO regulator*

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3.2 Transient Simulation

Fig. 8(a) shows the transient simulation of the proposed CLDO regulator at zero load and at the maximum load of 200 mA. From the waveforms, it is shown that the CLDO regulator regulates the output voltage V_{OUT} at 1.0 V and the feedback voltage V_{FB} of 0.4 V as expected, with a difference of 30 µV at maximum load for V_{OUT} and 110 µV at zero load for V_{FB}. The measured quiescent current from the simulation is 5.8 µA at maximum load and 5.18 µA at zero load as shown in Fig. 8(b). The single-digit micro-ranged quiescent current contributes greatly in achieving very low power consumption during the idle mode of the CLDO regulator which can be within single-digit micro-Watt range where ultra-low power applications such as energy-harvested devices operate. The transient simulation waveforms in Fig. 9 shows that the CLDO regulator is able to regulate the expected V_{OUT} and V_{FB} at various load currents ranging from 20 mA up to 200 mA with minimal output variation. Four low range load currents below 20 mA tested, 10 µA, 100 µA, 1 mA and 10 mA and for all four tested currents, the obtained outputs V_{OUT} and V_{FB} remained as expected. This shows that the proposed CLDO regulator is able to regulate the anticipated output voltage for a wide range of 0-200 mA load current. This is a noteworthy outcome as it is uncommon for a CLDO to achieve a maximum load current of up to 200 mA. This range is usually achieved by conventional LDO regulators with the presence of external output capacitors. The wide load range provides flexibility for the CLDO regulator to power either a low current load or a much larger load, expanding its availability for more variety of circuits to drive.

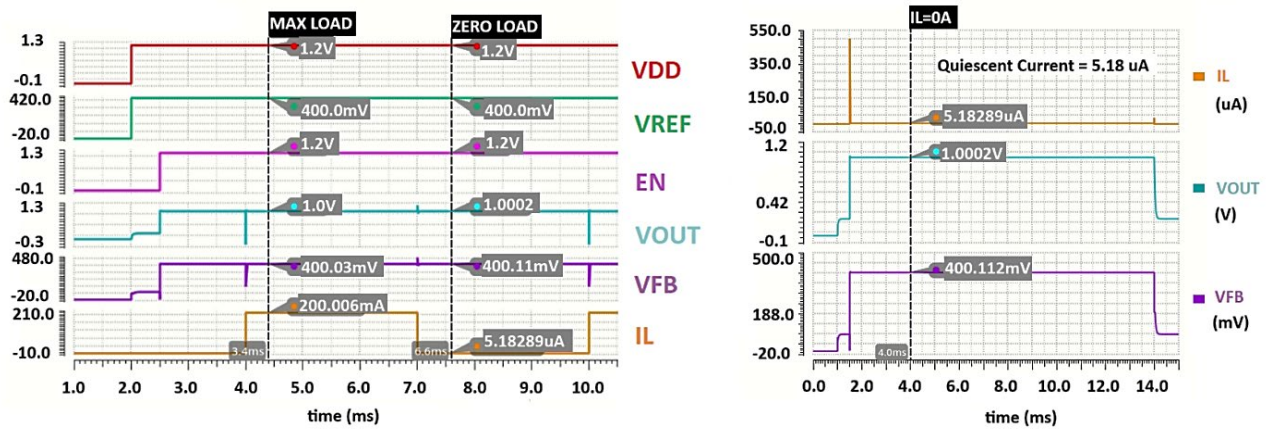

Fig. 8 *Transient simulation results with maximum load current (a) and quiescent current measurement; (b) of the proposed CLDO regulator*

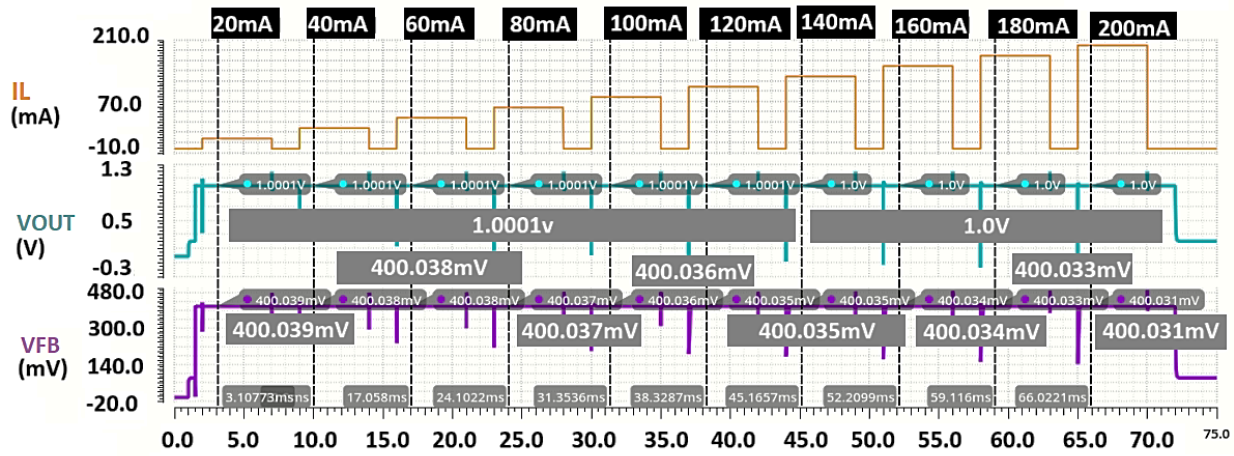

Fig. 9 *Transient simulation results for multiple load currents from 20 mA to 200 mA of the proposed CLDO regulator*

3.3 AC Analysis

The DC gain, phase margin and the unity gain bandwidth of the proposed CLDO at maximum load is shown in Fig. 10(a) and 10(b), with the values of 92 dB, 61.9° and 286 kHz respectively. The DC gain of 92 dB is notably high and the phase margin of 61.9° depicts that the proposed CLDO regulator operates in the stable range at its maximum load current. The PSRR curves of the CLDO regulator are plotted for four different load currents at three different frequencies and are shown in Fig. 11. The highest PSRR at 10 Hz is given by 150 mA load current, while the maximum load current of 200 mA PSRR is -77 dB. The PSRR degrades at 1 kHz with the values around 65±1 dB for all four load currents. The proposed CLDO regulator works with acceptably high PSRR at low frequency range between 1 Hz to 1 kHz.

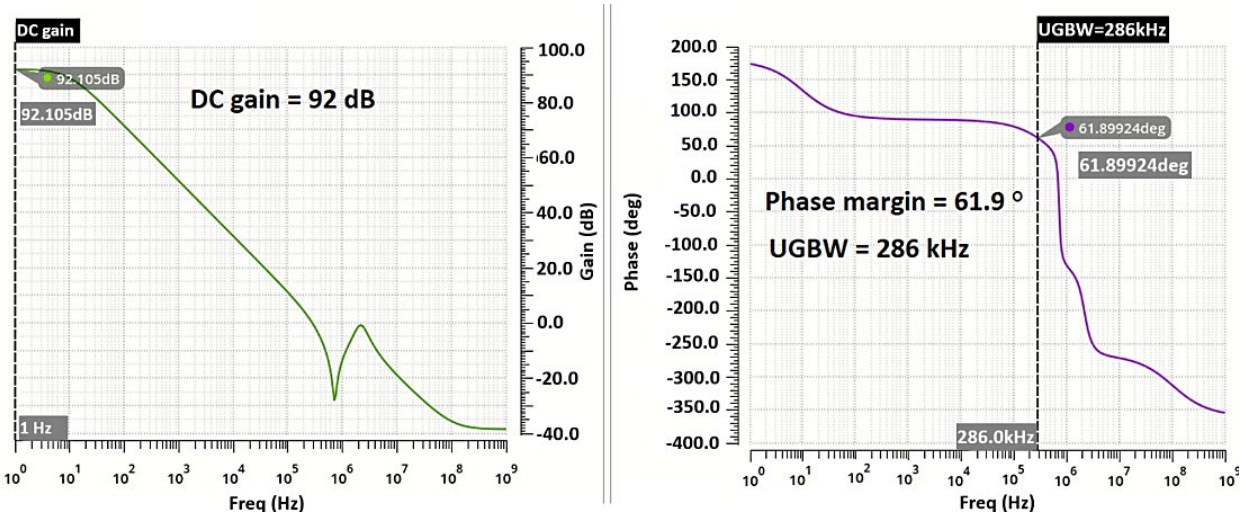

Fig. 10 *DC gain (a) UGBW and phase margin; (b) of the proposed CLDO regulator*

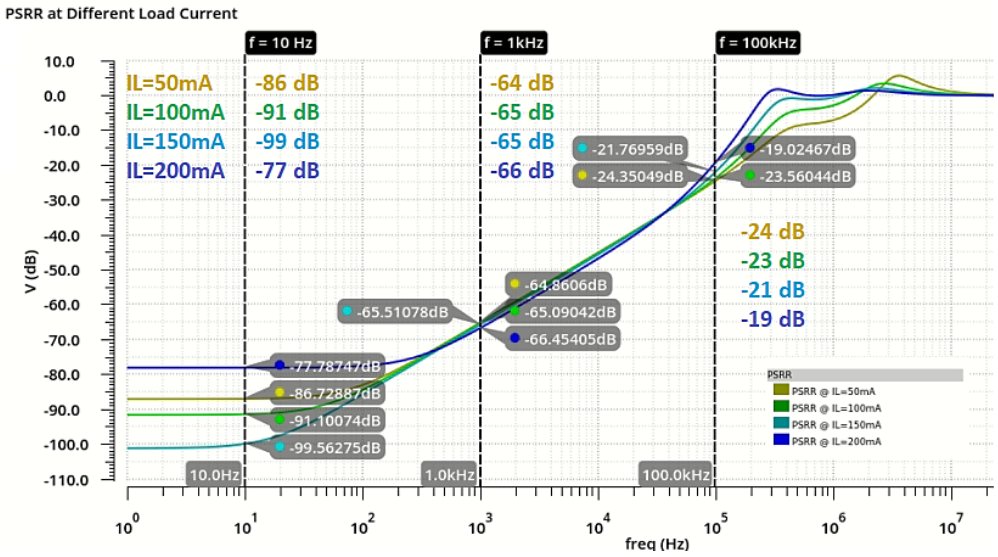

Fig. 11 *PSRR of the proposed CLDO regulator at different load currents*

3.4 Summary of Results

The overall specifications and simulation results of the proposed CLDO regulator are summarized in Table 1, including selected prior works with the same input and output voltage characteristics for comparison. From the table, the dropout voltage of the proposed CLDO regulator is 0.1 V much lower than the rest of the others with an

80% improvement from the OCL LDO. The load current range of the proposed CLDO is also doubled to the rest of the prior works. The achieved quiescent current of 5.8 µA is better than prior works for maximum cases.

Table 1 *Summary of results of proposed CLDO regulator and prior work comparison*

Parameter	TCASI (2012)	TCASII (2013)	OCL LDO (2018)	**This Work (2023)**
CMOS Technology (nm)	65	350	180	110
Input Voltage (V)	1.2	1.2	1.2	1.2
Output Voltage (V)	1	1	1	1
Dropout Voltage (V)	0.2	0.2	0.2	0.1
Max Load Current (mA)	100	100	100	**200**
Line Regulation (mV/V)	4.7	NA	0.283	**0.056**
Load Regulation (mV/mA)	0.3	NA	0.077	0.11
PSRR (I_{LMAX}) (dB@Hz)	-58 @ 10k	NA	-37.7 @ 1M	-66 @ 1k
Quiescent Current (µA)	0.9_{min}, 82.4_{max}	1.2_{min}, 14_{max}	0.407_{min}, 245_{max}	5.18_{min}, $\mathbf{5.8}_{max}$

4. Conclusion

A 5.18 µA low quiescent current 110 nm CLDO regulator operating at a nominal voltage of 1.2 V regulating the output voltage of 1.0 V with a wide load current range of up to 200 mA and 80% line transient improvement is designed and simulated. The single-digit micro-ranged quiescent current greatly contributes in minimizing power consumption during the idle mode of the CLDO regulator which can be within single digit micro-Watt range where ultra-low power applications operate, thus prolonging the battery life, whilst the wide load range provides flexibility for the proposed CLDO regulator to power a larger range of circuits to drive with better line regulation and relatively good PSRR at low-frequency range.

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Conflict of Interest

Authors declare that there is no conflict of interest regarding the publication of the paper.

Author Contribution

The authors confirm their contribution to the paper as follows: ***study conception and design:*** *Wan Maziyah Ab. Halim;* ***data collection:*** *Wan Maziyah Ab. Halim;* ***analysis and interpretation of results:*** *Wan Maziyah Ab. Halim, Yuzman Yusoff;* ***draft manuscript preparation:*** *Wan Maziyah Ab. Halim, Julie Roslita Rusli, Suhaidi Shafie, Suraya Shaban. All authors reviewed the results and approved the final version of the manuscript.*

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