UNIVERSITI PUTRA MALAYSIA

THE DESIGN OF LOW POWER CMOS SRAM SUBSYSTEMS

LEE CHU LIANG

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By

LEE CHU LIANG

Thesis Submitted in Fulfilment of the Requirement for the Degree of Master of Science in the Faculty of Engineering Universiti Putra Malaysia

June 2001

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

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June 2001

Chairman : Encik Rahman Wagiran

Faculty : Engineering

The low power circuit design technique has been the trend in developing portable and smaller size electronic products, especially for communication peripherals. In the limitation on the device technology, integrated circuit design work has played an important role in performing various low power techniques. This thesis presents the design of low power Complementary Metal Oxide Semiconductor (CMOS) Static Random Access Memory (SRAM) Subsystems. CMOS technology performs much lower static power dissipation compares to other technologies. The implementation of this design by using 3.3 V supply voltage has effectively reduced the dynamic power dissipation of the circuitry. Low power is achieved by implementing 6T-memory cell. Low power techniques are also achieved on capacitance reduction by using divided word-line structure for address decoder. Finally the low power is achieved by the operating voltage reduction using current-mode sensing technique for sense amplifier with the pre-charge voltage of $V_{dd}/2$.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
Sebagai memenuhi keperluan untuk ijazah Master Sains

REKABENTUK CMOS SUBSISTEM SRAM BERKUASA RENDAH

Oleh

LEE CHU LIANG

Jun 2001

Pengerusi : Encik Rahman Wagiran

Fakulti : Kejuruteraan

Teknik rekabentuk untuk litar berkuasa rendah telah menjadi satu amalan dalam pembangunan barangan elektronik yang mudah alih dan bersaiz kecil terutamanya bagi alat komunikasi. Semakin teknologi peranti mencapai hadnya, rekabentuk litar bersepadu menjadi semakin penting dalam usaha untuk mempelbagaikan teknik untuk litar berkuasa rendah. Tesis ini akan menyampaikan rekabentuk Complementary Metal Oxide Semiconductor (CMOS) Subsistem Static Random Access Memory (SRAM) berkuasa rendah. Teknologi CMOS kurang kehilangan kuasa statik berbanding dengan teknologi lain. Implementasi rekabentuk litar ini dijalankan dengan menggunakan 3.3V sebagai sumber voltan yang telah secara berkesan mengurangkan kehilangan kuasa dinamik litar tersebut. Kuasa rendah boleh dicapai dengan menggunakan sel ingatan 6T. Teknik berkuasa rendah juga boleh dicapai menggunakan pengurangan kapasitan dengan menggunakan struktur pembahagi baris untuk pengkodan alamat. Akhirnya kuasa rendah boleh dicapai dengan penggurangan voltan operasi dengan menggunakan teknik pengesan secara mod arus untuk penguat-kesanan dengan pra-cas bervoltan V_{dd}/ 2.

ACKNOWLEDGEMENTS

A sincere appreciation is delivered to my project supervisors Mr. Rahman Wagiran, Dr. Bambang Sunaryo Suparjo and Dr. Roslina Sidek for their invaluable guidance, constructive suggestions and encouragement throughout the duration of this project.

I also wish to extend my deepest personal thanks to my dearly course-mates to whom I owe my sincere appreciation. They are W. B. Puah, G. H. Tan, Lini Lee and Philip Tan which have indeed made my project more interesting and meaningful.

Lastly, I would like to express my sincere appreciation to my family for their undying love, patience and supports which have enable me to complete the project successfully.

I certify that an Examination Committee met on 15th June 2001 to conduct the final examination of Lee Chu Liang on his Master of Science thesis entitled "The Design of Low Power CMOS SRAM Subsystems" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulation 1981. The committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committees are as follows:

NASRULLAH KHAN, Ph.D.
Faculty of Engineering,
Universiti Putra Malaysia
(Chairman)

RAHMAN WAGIRAN, MSc.
Faculty of Engineering,
Universiti Putra Malaysia
(Member)

BAMBANG SUNARYO SUPARJO, Ph.D.
Faculty of Engineering,
Universiti Putra Malaysia
(Member)

ROSLINA SIDEK, Ph.D.
Faculty of Engineering,
Universiti Putra Malaysia
(Member)

MOHD. GHAZALI MOHAYIDIN, Ph.D.
Professor/Deputy Dean of Graduate School,
Universiti Putra Malaysia.

Date: 12 JUN 2001

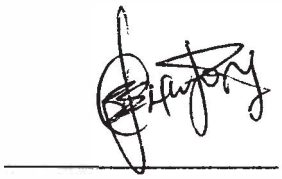
This thesis submitted to the Senate of Universiti Putra Malaysia has been accepted as fulfilment of the requirement for the degree of Master of Science.

AINI IDERIS, Ph.D.
Professor/Dean of Graduate School
Universiti Putra Malaysia

Date:

DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.



(LEE CHU LIANG)

Date: 21/6/2001

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LIST OF ABBREVIATIONS

4T cell	Four transistors memory cell
6T cell	Six transistors memory cell
C_d	Drain capacitance
C_g	Gate capacitance
C_L	Load capacitance
C_{ox}	Capacitance oxide
CMOS	Complementary Metal Oxide Semiconductor
DWL	Divided Word-Line
Gnd	Ground
GWD	Global Word Decoder
I_D	Drain current
K_n	NMOS Transconductance coefficient
K_p	PMOS Transconductance coefficient
L	Channel Length
LWD	Local Word Decoder
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-channel Metal Oxide Semiconductor
PMOS	p-channel Metal Oxide Semiconductor
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
V_{dd}	Supply voltage
VTC	Voltage Transfer Curve
V_t	MOSFET Threshold voltage
W	Channel Width
β	Taper factor
β_{eff}	MOSFET process gain factor
τ	Time constant

CHAPTER 1

INTRODUCTION

The Design of Low Power SRAM

The low power Static Random Access Memory (SRAM) integrated circuit design technique has always been the trend in developing portable electronic products. With the demand on reducing weight and size of portable system, instead of miniaturizing the batteries, designing low power digital systems has become a more practical step. With memory accounting for the largest share of power consumption in a system, circuits designing techniques are a leading field with device technology constraint.

SRAM is a volatile memory in which data in the memory will disappear when power supply is turned off. A latch structure is used in the SRAM memory cell to store data. More transistors are needed in the SRAM memory cell compare with a DRAM which is based on dynamic storage of charge for data storage. Today's industry uses SRAM especially as memory cache mainly because of its speciality in high speed for read and writes operations.

Figure 1.1 shows the floorplan of the SRAM subsystems design in this work. The memory cell arrays are divided into four similar portions with modules in between. Pre-decoder and global row decoders are placed in the center column.

Column decoders, sense amplifier, write drivers and I/O buffers are placed in the center horizontal area.

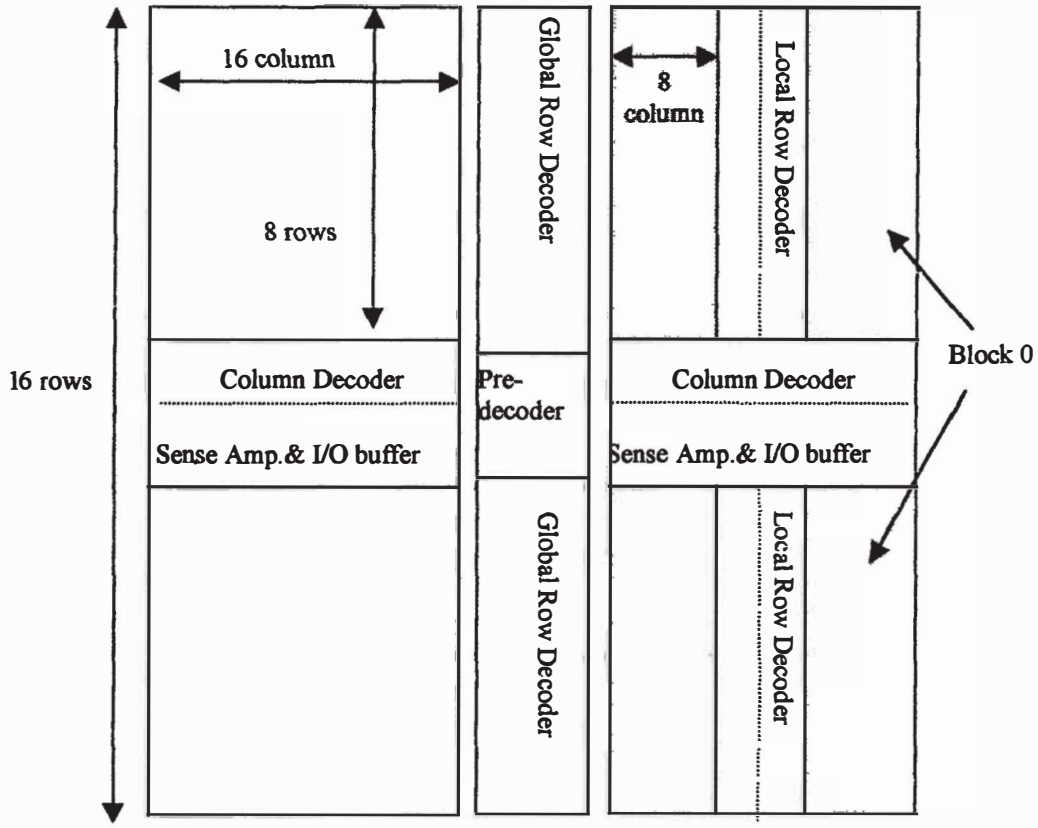

Figure 1.1: Floorplan of 512 x 8-bits low power SRAM subsystems.

The emphasis on this work is mainly on the design of memory cell, address decoder and the sensing amplifier. For each of these subsystems, low power techniques have been reviewed and the suitable techniques are adopted in this work.

Low power consideration will subsequently lead to the deterioration of the system performance especially in delay parameter. Since the main justification for the existence of the SRAM is its speed, thus the low-power circuit design techniques used in this work are to be concerned and compromised with its high-speed performance. The design work is carried out using Tanner Tools Pro. using SPICE simulation. The design flow is shown in Figure 1.2. The design work of the 512 x 8-bits low density SRAM subsystems has indeed a great gain in obtaining basic knowledge of circuit design skills and techniques. The variety of proposed circuit design techniques in designing the low power SRAM Subsystems has also a perfect reference for a beginner to step in the world of art of the integrated circuit design.

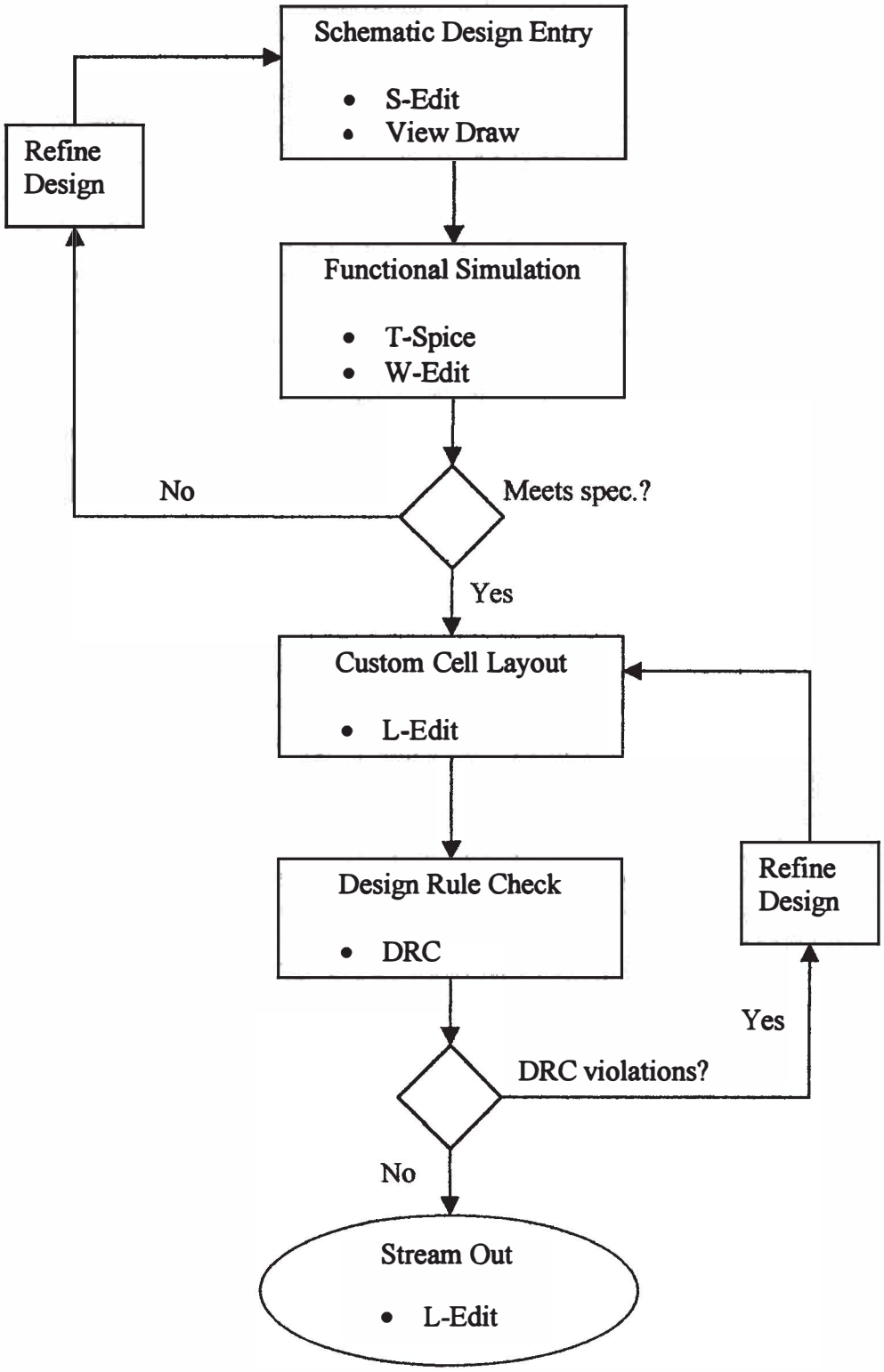

Figure 1.2: Design Flow using Tanner Tools

Circuit Limitation of Low Power VLSI Design

The circuit level limits are independent of the architecture of a particular system. There are a few circuit level limits for CMOS technology. The first generic circuit limit is the supply voltage. Reducing supply voltage is the most effective way of decreasing dynamic power dissipation in CMOS circuit. However the minimum supply voltage is determined by the minimum threshold voltage by a simple equation (Luo and Kuo,1999) which is

$$V_{dd,\min} = 3V_{T,\min} \qquad \ldots 2.1$$

In this work, lower voltage 3.3 V is chosen instead of 5 V. With reference to the available technology model file, supply voltage 3.3 V still fulfills the requirement of the Equation 2.1. Further more, lower power supply voltage will significantly reduce the speed of operation. This is because the increase in the gates' transition time is inversely proportional to the supply voltage, as in Equation 2.2. where k is the process constant, $\beta_{p/n}$ is the process gain factor and C_L the load capacitance.

$$t_{r/f} = k\left(\frac{C_L}{\beta_{p/n}V_{dd}}\right) \qquad \ldots 2.2$$

The second generic circuit limit is the switching frequency. The dynamic power dissipation is

$$P = \frac{1}{2}C_L V_{dd} f \qquad \ldots 2.3$$

The highest frequency devices are used but operating them at the lowest possible frequency.

The third limitation is on the intrinsic gate delay that is the time taken to charge or discharge the load capacitance. With the available technology model file, this problem can be overcome by using less fan-out with minimum geometry.

Objective of This Work

Low power techniques has been one of the challenges today in producing portable and smaller electronics products. SRAM being one of the most high power consumption products will be the first front priority to be studied. In this work, low power techniques are studied by using available technology.

The objectives of this thesis is to present the circuit design of CMOS SRAM subsystems using low power techniques and further develops its physical layout by using available MOSIS/ ORBIT 2.0µm Level 2 CMOS technology. Implementation of this design by using 3.3 V supply voltage is to reduce the dynamic power dissipation of the whole circuitry. Studies are made on three subsystems of SRAM as below:

a) Implementation of low power 6T-memory cell.

b) Low power technique implementation on capacitance reduction by using divided word-line structure for address decoder.

c) Implementation of current sense amplifier with the pre-charge voltage of $V_{dd}/2$.

The benefits of this design work will be the valuable knowledge and circuit design experience. In terms of contribution, this work can be a valuable learning reference in circuit level design work.

Thesis Organization

This thesis comprises of five chapters. Chapter 1 gives an overview to this project being done. The limitations of the circuit level design are discussed and the objectives of this work are mentioned. Chapter 2 presents the literature review which discusses the related research work had been done previously. Chapter 3 discusses the methodology involved in this design work. The theory of the origin of power dissipation in CMOS is also presented.

The scope of this project will be captured in three subtitles in Chapter 3. These subtitles are discussing memory cell, address decoder and sense amplifier, which are three of the core part of SRAM architecture. The detail description of the technique and structures used are also presented. The results obtained are then discussed in Chapter 4. Finally, Chapter 5 will conclude the work.

CHAPTER 2

LITERATURE REVIEW

CMOS Technology

CMOS circuits have been the forefront of the technology due to their low passive power consumption. Aside from leakage currents, power in CMOS circuit is only dissipated during switching events. Virtually no power consumed when the circuit is in the steady state. Figure 2.1 shows gate delay versus power consumption of various logic families (Kohyama, 1990). At a power-delay product value, CMOS offers the smallest power-delay product among all available technology.

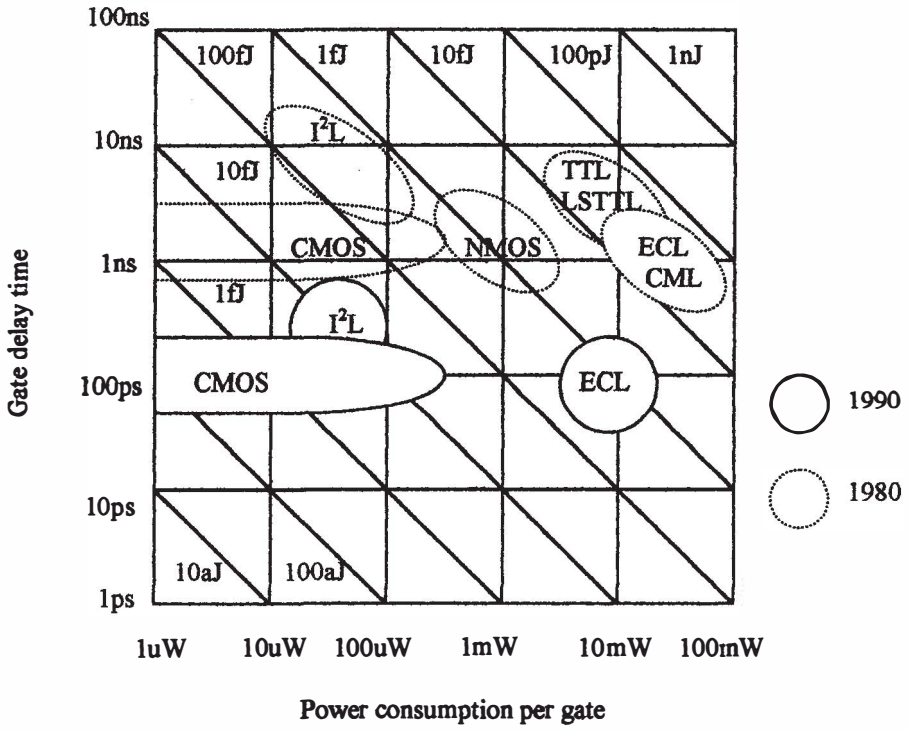

Figure 2.1: Gate delay versus power consumption of various logic families (Kohyama, 1990).

In addition, CMOS is flexible for a wide variety of design applications, which include digital logic, signal processing and a variety of analog circuits. The significant features of CMOS with its stable operation have further permitted varieties of CMOS IC to be fabricated with high yield.

As a result of today's technology, it is widely accepted that power efficiency is a design goal at par in importance with miniaturization and performance. Therefore, the practice of low power design is being adopted and dominated by the CMOS technology.

Development of Low Power SRAM

Memory circuits form an integral part of every system design and significantly contributing to the system level power consumption. Two examples of recently presented reduced-power processors show that 43% and 50.3% respectively of the total system consumption is attributed to the memory circuits (Stephany et al., 1998; Igura et. al., 1998). Therefore, reducing the power dissipation in memories can significantly improve the system power-efficiency, performance, reliability and overall costs.

The main justification for the existence of SRAM is its speed since it consumes a quarter of the area capacity of DRAM for the same process technology and chip size. The bandwidth mismatch is better between microprocessor and the

SRAM than the DRAM. A rapid growing classification of fast memory architecture is the Synchronous SRAM especially used as the cache in PC systems. With the rapid development in VLSI fabrication technology that has led to the increased densities of integrated circuits with the decreased device geometry, low supply voltage have effectively reduces the excessive power dissipation and decreases run time failure and reliability problems. SRAM has experienced a very rapid development of low power design due to an increased demand for notebooks, laptops, hand-held communication devices and IC memory cards.

Address Decoder

Researches had been made on the reduction of power consumed during word-line activation. Divided word-line (DWL) approach has been the most preferable because of its effectiveness in reducing load and save unused power (Yoshimoto, 1983). It is commonly used especially in an increasing density of memory array size. In the further extend of DWL architecture, the hierarchical word-line decoding (HWD) technique is used for higher density SRAM (Hirose et. al., 1990). This architecture has three layer hierarchy which includes the global word-lines, sub-global word-lines, and local word-lines. Other than this, the technique using hierarchical divided bit-line that results in the reduction in the bit-lines capacitance instead of word-lines capacitance had been presented recently (Karandikar, 1998). This architecture uses slightly different memory cell's structure in which it used single bit-line and double word-line. However, in this work, divided word-line is used due to the small density of the memory cell array.