UNIVERSITI PUTRA MALAYSIA

AN EFFICIENT ARCHITECTURE OF 8-BIT CMOS ANALOG-TO-DIGITAL CONVERTER

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2000

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By

PHILIP TAN BEOW YEW

Thesis Submitted in Fulfilment of the Requirement for the Degree of Master of Science in the Faculty of Engineering Universiti Putra Malaysia

December 2000

DEDICATION

To my family,

Father (Edward), mother (Elaine), sister (Margaret),

and my wife,

Christine

Abstract of thesis presented to the Senate of Universiti Putra Malaysia
in fulfilment of the requirement for the degree of Master of Science.

**AN EFFICIENT ARCHITECTURE OF
8-BIT CMOS ANALOG-TO-DIGITAL CONVERTER**

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PHILIP TAN BEOW YEW

November 2000

Chairman : Dr. Bambang Sunaryo Suparjo

Faculty : Engineering

An 8-bit CMOS analog-to-digital converter (ADC) has been designed by using a more efficient architecture, which is known as the simplified multistep flash architecture. This architecture can ultimately reduce the number of comparators needed in an ADC. For the same resolutions, the full-flash architecture requires 255 comparators; the half-flash architecture requires 30 comparators, but the new architecture needs only six comparators. For conversion speed, the half-flash architecture has about half the speed of the full-flash architecture, but the comparator counts for the half-flash architecture is greatly reduced compared to the full-flash architecture. While, for the simplified multistep flash architecture, even though the comparator counts is very much reduced compared to the half-flash architecture, but the conversion speed of the new architecture is still the same as that of the half-flash architecture.

In order to design this new ADC, the entire architecture is divided into six separate parts. The suitable computer aids for designing and doing simulation are

employed at the beginning of the design process. In this project, the integrated circuit design program from Tanner Research, Inc. is used for designing from the system level to the layout level. The simulation results show that the conversion rate of this new architecture is 111 kHz, while the differential non-linearity (DNL) and integral non-linearity (INL) of this architecture are both ±1.19 LSB (least significant bit). This is due to the elimination of three digital codes of the conversion system. By ignoring these three missing codes, the new ADC is estimated to have not more than ±1.00 LSB of DNL and INL values.

The mask layout diagram that is used for fabrication purpose is also successfully developed in this project. Although, the simulation results from the layout diagram indicate the system has lower accuracy compared to the expected results from the schematics, the conversion from an analog voltage to eight digital bits, is successfully achieved. The full-custom approach is chosen in designing the layouts because it provides complete design freedom to the designer.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Master Sains

SATU SENIBINA CEKAP BAGI PENUKAR ANALOG-KEPADA-DIGIT CMOS 8-BIT

Oleh

PHILIP TAN BEOW YEW

November 2000

Pengerusi : Dr. Bambang Sunaryo Suparjo

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Satu penukar analog-kepada-digit (ADC) CMOS 8-bit telah direkabentuk dengan menggunakan satu senibina yang cekap, yang dikenali sebagai senibina kilat pelbagai langkah teringkas. Senibina ini dapat mengurangkan bilangan pembanding yang diperlukan dalam satu ADC dengan sangat berjaya. Bagi resolusi yang sama, senibina kilat-penuh memerlukan 255 pembanding; senibina kilat-separuh memerlukan 30 pembilang, tetapi senibina baru ini hanya memerlukan enam pembanding. Bagi kelajuan penukaran, senibina kilat-separuh mempunyai hampir setengah daripada kelajuan senibina kilat-penuh, tetapi bilangan pembilang bagi senibina kilat-separuh telah banyak dikurangkan berbanding dengan senibina kilat-penuh. Manakala bagi senibina kilat pelbagai-langkah dipermudah, walaupun bilangan pembilang telah banyak dikurangkan berbanding dengan senibina kilat-separuh, tetapi kelajuan penukaran bagi senibina baru masih sama dengan yang senibina kilat-separuh.

Bagi merekabentuk ADC yang baru ini, seluruh senibina dibahagikan kepada enam bahagian yang berasingan. Kemudahan komputer yang sesuai untuk merekabentuk dan melakukan simulasi didapatkan pada permulaan proses merekabentuk. Dalam projek ini, program merekabentuk litar terkamir daripada Tanner Research, Inc. digunakan untuk merekabentuk dari peringkat sistem hingga ke peringkat bentangan. Keputusan simulasi menunjukkan bahawa kadar penukaran bagi senibina baru ini ialah 111 kHz, manakala kedua-dua pembezaan tidak-seragam (DNL) dan pengkamilan tidak-seragam (INL) bagi senibina ini adalah ±1.19 LSB (bit paling tidak penting). Ini adalah disebabkan oleh penghapusan tiga kod digit pada sistem penukaran. Dengan mengabaikan ketiga-tiga kod yang hilang ini, ADC baru ini dijangkakan mempunyai nilai DNL dan INL yang tidak lebih daripada ±1.00 LSB.

Gambarajah topeng bentangan yang digunakan untuk tujuan fabrikasi juga berjaya dihasilkan dalam projek ini. Walaupun keputusan simulasi daripada gambarajah bentangan menunjukkan sistem mempunyai ketepatan yang lebih rendah berbanding dengan keputusan jangkaan daripada skematik, tetapi penukaran daripada satu voltan analog kepada lapan bit digit dapat dicapai dengan jayanya. Kaedah "full-custom" dipilih dalam merekabentuk lapisan-lapisan bentangan ini kerana ia memberikan kebebasan merekabentuk yang menyeluruh kepada perekabentuk.

ACKNOWLEDGEMENTS

Firstly, I would like to express my utmost gratitude to my project supervisor, Dr. Bambang Sunaryo Suparjo (Head, Department of Electrical and Electronic Engineering, Universiti Putra Malaysia) and my supervisory committee, Dr. Roslina Sidek and Mr. Rahman Wagiran for their invaluable advice, guidance, constructive suggestions and encouragement throughout the duration of this project.

A sincere thanks goes to Prof. Dr. Dipankar Nagchoudhuri (Head, Department of Electrical Engineering, Indian Institute of Technology, Delhi) for his unconditional guidance, which enable me to solve most of the obstacles in both my studies and my research project. I am extremely grateful to my supportive group of friends, Puah Wei Boo, Lini Lee, Tan Gim Heng and Lee Chu Liang, who have help me a lot to complete my project successfully. Special thanks goes to Mr. Nasri Sulaiman and all the staff of the Electrical and Electronic Department, Universiti Putra Malaysia for their sincere help and co-operation. Not forgetting also, to all my lecturers, thanks for everything.

Finally, I would like to express my sincere thanks to my beloved family, my wife (Christine), my course mates and all my friends for their undying love and support that had enable me to deal with hard work and difficulties patiently.

I certify that an Examination Committee met on 22 December 2000 to conduct the final examination of Philip Tan Beow Yew on his Master thesis entitled "An Efficient Architecture of 8-bit CMOS Analog-to-digital Converter" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulation 1981. The Committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

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This thesis submitted to the Senate of Universiti Putra Malaysia has been accepted as fulfilment of requirement for the degree of Master of Science.

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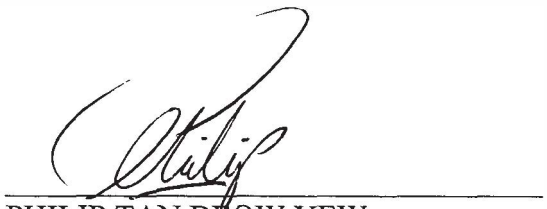
DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.



PHILIP TAN BEOW YEW

Date: 23 · 12 · 2000

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ADC	Analog-to-digital Converter
C	Capacitance
C_c	Compensation Capacitance
Clk	Clock
clr	Clear
CMOS	Complementary Metal Oxide Semiconductor
C_{ox}	Oxide Capacitance
DAC	Digital-to-analog Converter
DC	Direct Current
DFF	Delay Flip-flop
DFT	Design for Testability
DNL	Differential Non-Linearity
DSC	Digital Switch Control
Gnd	Ground
IC	Integrated Circuit
I_D	Drain Current
INL	Integral Non-Linearity
INT	Integer
L	Length
L-Edit	Layout Editor
LSB	Least Significant Bit
LSI	Large Scale Integration
LVS	Layout versus Schematic
M	MOS Transistor
MOSFET	Metal Oxide Field Effect Transistor
MSB	Most Significant Bit
MSI	Medium Scale Integration
Mux	Multiplexer

N_c	Comparator Count
NMOS	N-type MOS
Op-amp	Operational Amplifier
PC	Preset and Clear
PCM	Pulse Code Modulation
PMOS	P-type MOS
pre	Preset
Q	Output of the Latch
QBar	Complement of Q
Q_M	Output of the master-latch
R	Resistance
R_S	Sheet Resistance
S-Edit	Schematic Editor
SPICE	Simulation Program with Integrated Circuit Emphasis
SSI	Small Scale Integration
TFF	Toggle Flip-flop
TSPICE	Tanner SPICE
ULSI	Ultra Large Scale Integration
V^+	Positive voltage source
V^-	Negative voltage source
V_D	Drain Voltage
Vdd	Operating voltage source
V_{DS}	Drain-source Voltage
VE	Voltage Estimator
V_F	Feedback Voltage
V_G	Gate Voltage
V_{GS}	Gate-source Voltage
V_{in}	Analog input voltage
VLSI	Very Large Scale Integration
V_R	Reference voltage
$V_{R(LSB)}$	Reference voltage for second conversion cycle
$V_{R(MSB)}$	Reference voltage for first conversion cycle

V_S	Source Voltage
V_{SG}	Source-gate Voltage
V_{tap}	Voltage tap from the resistors ladder
V_{Tn}	Threshold Voltage for NMOS transistor
V_{Tp}	Threshold Voltage for PMOS transistor
W	Width
W-Edit	Waveform Editor
ε	Permittivity of dielectric material
μN	Mobility of electron in NMOS transistor
μP	Mobility of holes in PMOS transistor

CHAPTER 1

INTRODUCTION

What is Integrated Circuit?

Integrated circuit (IC) is the enabling technology for a whole host of innovative devices and system that have changed the way we live. Integrated circuits are much smaller and consume less power than the discrete components used to build electronic systems before the 1960s. Integration allows us to build systems with many transistors that allow more computing power to be applied for problem solving. Integrated circuits are also easier to design and manufacture and are more reliable than discrete system.

The growing sophistication of applications continually pushes the design and manufacturing of integrated circuits and electronic systems to new levels of complexity. The number of transistors per chip increases exponentially with time due to the minimum dimension of transistor has dropped from about 25 μm in year 1960 to about 0.18 μm in year 2000, resulting in a tremendous improvement in the speed of integrated circuits [1]. Analog, digital or mixed signal integrated circuits containing tens of thousands of devices, now routinely appear in consumer products.

Integrated circuits have three key advantages over digital circuits built from discrete components [2]:

1. **Size.** Integrated circuits are much smaller, that is both transistors and wires are shrunk to micrometer sizes, compared to the millimetre or centimetre scales of discrete components. Small size leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances and inductances.

2. **Speed.** Signals can be switched between logic 0 and logic 1 much quicker within a chip than between chips. Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board. The high speed of circuits on-chip is due to their small size, that is smaller components and wires have smaller parasitic capacitances to slow down the signal.

3. **Power consumption.** Logic operations within a chip also take much less power. Once again, lower power consumption is largely due to the small size of circuits on the chip, that is smaller parasitic capacitances and resistances require less power to drive them.

Why Focus on CMOS Technology?

In early 1960s, only n-type transistors were being produced. It was in the mid-1960 that Complementary Metal Oxide Semiconductor (CMOS) device, which is the combination of both n-type and p-type transistors, was introduced [1].

CMOS technology rapidly captured the digital market. This is because the CMOS gates only dissipated power during switching. It was soon discovered that the dimensions of Metal Oxide Semiconductor (MOS) devices could be scaled down more easily than other types of transistors.

The next obvious step was to apply CMOS technology to analog design. The low cost of fabrication and the possibility of placing both analog and digital circuits on the same chip have made CMOS technology an attractive technology. Although CMOS technology was slower than bipolar technology, the analog market is dominated by CMOS technology. This is due to device scaling that has improved the speed of MOS transistors by more than three orders of magnitude in the past 30 years, becoming comparable with that of bipolar devices, even though the latter have also been scaled down but not as fast as the MOS devices.