UNIVERSITI PUTRA MALAYSIA

DEVICE CHARACTERIZATION OF 0.8-µm CMOS TECHNOLOGY

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Thesis Submitted in Fulfilment of the Requirements for the Degree of Master of Science in the Faculty of Engineering Universiti Putra Malaysia

May 2000

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirements for the degree of Master of Science.

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May 2000

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The development of the 0.8-μm CMOS technology was carried out in Mimos Berhad and is considered to be the first in-house development to be done in Malaysia. In every technology development, characterization of the technology is always necessary to gauge its performance and reliability. This thesis is a result of such work and the emphasis of the characterization is the devices of 0.8-μm CMOS technology. The main work of this thesis includes the effort taken to understand the technology, the design of test structures and the development of test methodology to qualify the 0.8-μm CMOS technology. The test structures design includes the p-n junction, MOS enhancement transistor, thick oxide transistor and MOS capacitor.

The p-n junction was designed specifically to investigate the breakdown voltage of the source/drain of NMOS and PMOS, which is a very important parameter in determining the reliability of the devices. MOS enhancement transistor characteristics were examined in detail with the NMOS and PMOS test structures. Typical I-V characteristics and some important device parameters were obtained from the I-V characterization. Two main issues, i.e. threshold voltage variation and off state leakage current were discussed in detail. Test methodologies for effective

channel length determination (L_{EFF}), Drain-Induced Barrier Lowering (DIBL), punchthrough and Gate-Induced Drain Leakage (GIDL) are among the important ones that were developed. The isolation issues for the devices were addressed using the thick oxide transistors to obtain the high field threshold voltage (V_{TF}). The V_{TF} is used as a measure to show the absence of parasitic FET near the operating voltage of 5 V. The conventional MOS capacitor was also included as one of the test structures due to its simplicity and enormous amount of information that can be obtained. A detail capacitance-voltage (C-V) characterization was carried out using the Simultaneous Feedback Charge technique. Analysis includes the extraction of doping profiles, interface trap density (D_{it}) and some process information such as conductivity and gate oxide thickness (t_{ox}).

The work has shown a tremendous effort being put to design test structures and characterize the 0.8-μm CMOS devices. The test structures which designs are based on its predecessor, the 1.0-μm CMOS technology test structures, have proven to be reliable and capable. Based on the result analysis, it shows that the 0.8-μm CMOS devices have achieved a creditable performance and reliability. As a conclusion, this work have achieved its objective to design device test structures, develop the respective test methodology and to characterize the technology.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

PENCIRIAN PERANTI TEKNOLOGI 0.8-μm CMOS

Oleh

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Mei 2000

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Pembangunan teknologi CMOS 0.8-μm telah dijalankan di Mimos Berhad dan dipercayai adalah yang pertama di Malaysia. Pada kebiasaannya, untuk setiap pembangunan teknologi, pencirian adalah amat penting kerana ia diperlukan untuk mengukur prestasi dan ketahanan sesuatu teknologi. Tesis ini adalah hasil kerja tersebut dan keutamaan pencirian adalah kepada peranti CMOS 0.8-μm. Tujuan utama tesis ini merangkumi usaha gigih yang diluangkan untuk memahami teknologi, mereka struktur ujian peranti serta pembangunan metodologi ujian untuk melayakkan teknologi CMOS 0.8-μm. Struktur ujian yang direka termasuk simpangan p-n, transistor peningkatan MOS, transistor oxida tebal dan kapasitor MOS.

Struktur ujian simpangan p-n telah direka khusus untuk menyiasat voltan jatuhan punca/salir bagi peranti NMOS dan PMOS. Parameter ini adalah amat penting dalam menentukan ketahanan peranti. Pencirian transistor peningkatan MOS telah dilakukan ke atas rekaan struktur ujian peranti NMOS dan PMOS. Ciri-ciri I-V yang tipikal beserta dengan beberapa parameter peranti yang penting telah diperolehi melalui pencirian arus-voltan (I-V). Dua isu, iaitu perubahan voltan ambang dan

kebocoran arus keadaan diam telah diperiksa dengan terperinci. Antara metodologi ujian penting yang telah diketengahkan termasuklah penentuan panjang saluran efektif (L_{EFF}), kesan penurunan rintangan aruhan parit (DIBL), penembusan arus dan kesan kebocoran parit akibat aruhan get (GIDL). Isu pemencilan peranti telah disiasat dengan menggunakan rekaan transistor oxida tebal untuk mendapatkan voltan ambang medan tinggi (V_{TF}). Voltan ambang medan tinggi ini adalah merupakan ukuran yang memberikan indikasi bahawa parasit FET tidak wujud pada voltan operasi 5 V. Kapasitor MOS juga telah dipertimbangkan sebagai salah satu daripada struktur ujian disebabkan ia mudah serta mampu memberikan maklumat yang banyak. Pencirian jenis kapasitan-voltan (C-V) yang berasaskan teknik timbal-balas cas serentak telah dilakukan ke atas struktur yang direka. Analisis yang dilakukan termasuklah untuk mendapatkan profil pendopan, ketumpatan perangkap antara muka (D_{it}) dan beberapa maklumat proses seperti konduktiviti dan ketebalan get oxida (t_{ox}).

Pembangunan teknologi CMOS 0.8-μm ini telah memperlihatkan usaha gigih diperuntukan untuk mereka struktur ujian peranti, membangunkan metodologi ujian serta pencirian teknologi. Rekaan struktur ujian peranti yang berteraskan teknologi CMOS 1.0-μm telah membuktikan bahawa ia adalah berkesan dan boleh diharapkan. Berdasarkan analisis keputusan yang diperolehi, teknologi CMOS 0.8-μm ini telah memperlihatkan potensi yang memberangsangkan. Akhir sekali, boleh disimpulkan bahawa matlamat untuk mereka struktur ujian peranti, membangunkan metodologi ujian serta pencirian teknologi telah dicapai.

ACKNOWLEDGEMENTS

First and foremost, I would like to express my utmost gratitude to my project supervisors Dr. Bambang Sunaryo Suparjo, Dr. Mohd. Rais Ahmad and En. Rahman Wagiran for their invaluable guidance, constructive suggestions and encouragement throughout the duration of this project.

I am also extremely grateful to have a helpful and supportive group of friends and colleagues to whom I owe my sincere appreciation. They are H. T. Toh, Jeyakumar, Thiagesh, Zahrin, Ali, Esmat and K. P. Lim which have indeed made my project more interesting and meaningful. A special thanks also to En. Wan Mohd. Salleh, Vice President (Industry Development) of Mimos Berhad for giving me the opportunity and support throughout the duration of this project. Not forgetting also, the entire personnel of Wafer Fab, MySem which without them, this project will not materialize and remain a dream.

Lastly, I would like to thank my family and a very special friend of mine (Yee Ching) for their undying love, patience and support which have enable me to complete the project successfully. Thanks again for having faith in me!

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LIST OF ABBREVIATIONS

A	Area of capacitor
C_h	High frequency capacitance
C_q	Quasistatic frequency capacitance
C_{ox}	Capacitance oxide
D_{it}	Interface trap density
DIBL	Drain induced barrier lowering
GIDL	Gate induced drain leakage
g_m	Transconductance
I_D	P-N junction current
I_{DS}	Drain current
I_{DSt}	Subthreshold current
I_{DSat}	Saturation current
k	Boltzmann constant
L	Transistor length
L_M	Drawn channel length
L_{EFF}	Effective channel length
L_{VAR}	Different between the drawn and final length
L_{DIF}	Lateral diffusion of the source/drain implants
LOCOS	Local oxidation
MTI 1	Mimos test insert 1
N_A	Acceptor density
N_D	Donor density
n_I	Intrinsic carrier concentration
PATMOS	Parametric test for MOS devices
q	Electron charge
R_{TOT}	Total channel resistance
S_t	Subthreshold swing
SMU	Source measuring unit
t_{ox}	Gate oxide thickness
V_T	Threshold voltage
V_{TF}	High field threshold voltage
V_{BR}	Breakdown voltage
V_D	P-N junction voltage drop
V_{GS}	Gate voltage
V_{DS}	Drain voltage
V_{PT}	Punchthrough voltage
V_{DD}	Operating voltage
V_{SUB}	Substrate or bulk voltage
W	Transistor width
μ	Carrier mobility
μ_p	Hole carrier mobility
ε_{Si}	Silicon dielectric constant
τ	Absolute temperature
Φ_T	Built-in potential
Φ_{Fn}	Potential in the n-type region
Φ_{Fp}	Potential in the p-type region

CHAPTER 1

INTRODUCTION

Development of 0.8-μm CMOS Technology

The development of the 0.8-μm CMOS technology is the first to be initiated by Mimos Berhad in its bid to become a leading microelectronic center in Malaysia. The process flow of the technology development is as shown in Figure 1.1. The 0.8-μm CMOS technology development is based on the 1.0-μm CMOS technology obtained from a technology transfer in 1996. The origin of the technology is from the Fraunhofer Institute of Microelectronics and System, Germany.

The 0.8-μm CMOS technology development is a scaled down version of the 1.0-μm CMOS technology. The reason it is called a scaled down version is because the design rules are scaled linearly with different factor from the 1.0-μm CMOS technology. The constant voltage approach is implemented to maintain the operating voltage of 5 V. Factors that contribute to the feasibility of the scaled design rules are the equipment capability, device design and process integration issues. In terms of equipment capability, it is not so much of a problem because all equipment in Mimos Berhad is capable of processing up to the 0.5-μm at minimum. So, the limiting factor would be the device design and process integration. As devices are being scaled

down, many processes need to be modified in order to maintain the long channel characteristics and also to at least maintain or increase the reliability of the devices. Device design and process integration remains as an interesting challenge to be solved. However, it will not be discussed here because it is not within the scope of the thesis. The focus of this thesis will be the design of device test structures and its related characterization to qualify the 0.8-μm CMOS technology.

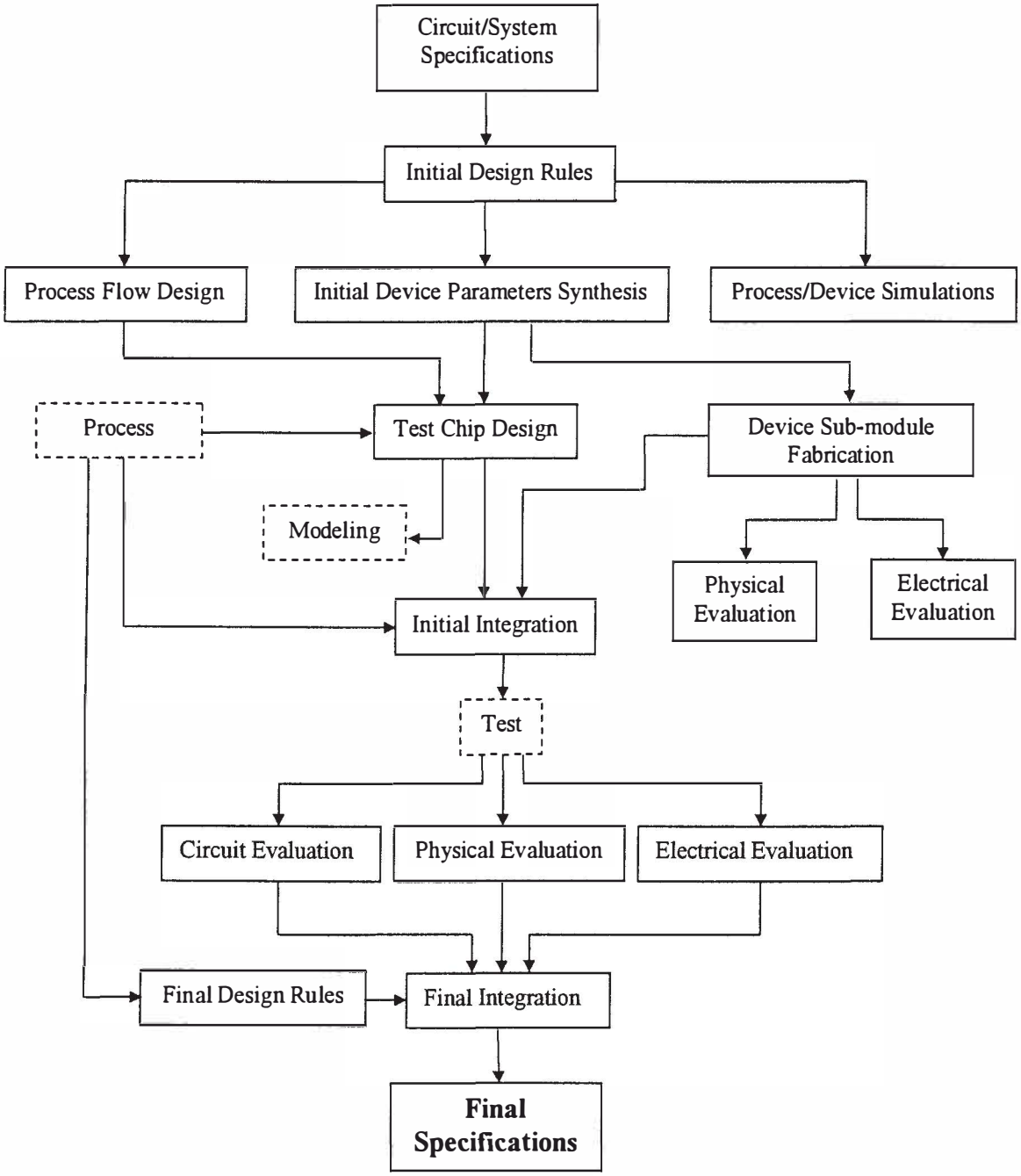

Figure 1.1: Process flow of the 0.8-μm CMOS technology development.

Scaling of Design Rules

Design rules or layout rules are description for preparing the masks or reticles used in the fabrication of integrated circuits (ICs). The rules serves as a necessary communication link between circuit designer and process engineer during the manufacturing phase. The main objective of the design rules is to obtain a design with optimum yield in as small an area as possible without compromising its reliability. Generally, design rules are a tradeoff between yield and performance. The more conservative the rules are, the more likely it is that the design will function but aggressive design rules will greatly enhance the performance of the design [1].

The challenge of present semiconductor trends would undoubtedly be the ability to increase the packing density of transistors. Downward transistor scaling allows an increase in circuit performance and packing density. The conventional scaling law states that if the physical dimension of a transistor is decreased horizontally and vertically, all by a factor of S (a value less than 1) and the operating voltage reduced by the factor of S^2, then gate delay will reduce by the same factor S and power per gate transition reduce by the factor of S^3 [2].

However, the conventional scaling law has not been always in favour because of certain constraints. The main one being the need to use the standard operating voltages. The modified version of the scaling law is termed "constant voltage" scaling. This approach shows that the transistor density and gate delay can be improved without scaling the voltage but the disadvantage being the non-scalable of some device design parameters such as electric field, leakage current and others.

Nonetheless, with a cautious device design approach, the constant voltage scaling was undertaken to develop the 0.8-μm CMOS technology design rules because of the desire to maintain the operating voltage of 5 V.

Design Rules for 0.8-μm CMOS Technology

The 0.8-μm CMOS technology design rules after a constant voltage scaling is implemented are given in Table 1.1 below.

Table 1.1: Design rules for 0.8-μm CMOS technology.

Description	Design Rule (μm)
n+ (p+) to p (n)-well distance	2.4
n+ and p+ width	1.5
n+ to p+ distance	1.3
Poly width	0.8
Poly overlap on n+ and p+	0.6
n+ and p+ width	1.5
Contact width	0.9
Contact to contact distance	0.45
Contact to poly distance	0.75
Contact overlap on n+, p+, poly and metal1	0.45
Via width	1.2
Via overlap on metal1 and metal2	0.45
Via to contact distance	0.9
Metal 1 width	1.0
Metal 1 distance	0.8
Metal 2 width	1.2
Metal 2 distance	0.9

Types of Test Structures

In the development of the 0.8-μm CMOS technology, there are basically six type of test structures in the test chip, MTI 1 (see Chapter 3), which are listed below:

1. Structures for process monitoring such as capacitors, transistors and diodes for oxide and junction breakdown.
2. Structures for the check of design rules such as minimum line width and metal pitch.
3. Structures for yield and reliability test such as contact and via chains.
4. Structures for extraction of model parameters such as transistors with varying width and length and sidewall capacitors.
5. Structures for failure analysis such as diodes with varying perimeter to area ratio and number of contacts for examining the diode leakage current.
6. Structures for non-electrical measurements such as optical and mechanical test.

In this thesis, the focus will be on the design and characterization of device test structures for the verification of 0.8-μm CMOS technology. Other test structures though important and complement the device test structures is not within the scope of this thesis. The test structures that will be discussed are listed below:

- P-N Junction (Diode)
- MOS Enhancement Transistors
- Thick Oxide Transistor
- MOS Capacitor