UNIVERSITI PUTRA MALAYSIA

RELIABILITY MODELING OF DYNAMIC THERMAL MANAGEMENT IN MULTICORE PROCESSOR

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RELIABILITY MODELING OF DYNAMIC THERMAL MANAGEMENT IN MULTICORE PROCESSOR

By

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

January 2018

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DEDICATIONS

This thesis is dedicated to my parents for their unconditional love, support, and encouragement. Also to my husband, the love of my life, a great soul mate and a big encouragement for all my moves in life. This way was so much harder to pass without them.

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Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirement for the degree of Doctor of Philosophy

RELIABILITY MODELING OF DYNAMIC THERMAL MANAGEMENT IN MULTICORE PROCESSOR

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January 2018

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With the continuous downscaling in semiconductor technology, the growing power density and thermal issues in multi-core processors are challenging and crucial. The system reliability associated with increased power dissipation affect the reliability of thermal management.

High temperatures and large thermal variations on the die create severe challenges in system reliability, performance, leakage power, and cooling costs. Dynamic thermal management (DTM) methods regulate the operating temperature based on the provided temperature profile from thermal sensors, which is transmitted using network-on-chip (NoC) in multi-core systems. DTM efficiency is highly dependent on the accuracy of thermal data.

Temperature profile inaccuracies are caused by various factors including sensor placement, sensor device imprecision, and interconnection deep sub-micron (DSM) noise. While temperature profile inaccuracies due to sensor placement and sensor device imprecision have been widely addressed, limited study performed on the impact of interconnection DSM noise on DTM efficiency. Hence, this thesis develops a comprehensive simulator model to investigate the impact of interconnect DSM noise on thermal data accuracy and DTM efficiency. The simulation results demonstrate that DSM noise severely affecting the MSbs of thermal data that leads to significant degradation of DTM performance.

To mitigate the DSM noise impact on DTM efficiency, an NoC fault tolerance scheme, exploiting inherent characteristics of DSM noise impacting the thermal data, is proposed that comparing to the standard coding scheme achieves lower cost in term of area and power consumption while increasing DTM efficiency by 38%.

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The second source of chip reliability involves power delivery network (PDN). PDN suffers from long-term reliability threats such as electro- migration (EM). Loss of limited Controlled Collapse Chip Connection (C4) pads to electro-migration makes delivering a stable supply voltage more critical. C4 bumps failure mechanism depends on current density, on-chip voltage noise, and temperature. In this thesis, the C4 bumps failure mechanisms dependency on each individual bumps' temperature value is explored that leads to more accurate mean-time-to-failure (MTTF) of the whole system. The simulation results demonstrate that using uniform temperature leads underestimating the system MTTF by up to 16 times due to exponentially dependency of C4 bump failure to temperature.

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Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

PEMODELAN KEBOLEHPERCAYAAN PENGURUSAN TERMA DINAMIK DALAM PEMPROSES BERBILANG TERAS

Oleh

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Dengan penskalaan rendah berterusan dalam teknologi semikonduktor, isu-isu peningkatan ketumpatan kuasa dan terma dalam pemproses berbilang teras adalah penting dan mencabar. Kebolehpercayaan sistem yang dikaitkan dengan peningkatan pelesapan kuasa boleh memVpengaruhi kebolehpercayaan pengurusan terma.

Suhu tinggi dan variasi terma yang besar pada die mewujudkan cabaran yang teruk dalam kebolehpercayaan sistem, prestasi, kuasa bocor, dan kos penyejukan. Pengurus DTM mengawal suhu operasi berdasarkan profil suhu yang disediakan dari sensor terma, yang dihantar menggunakan rangkaian-atas-cip (NoC) dalam sistem berbilang teras. Kecekapan adalah DTM sangat bergantung kepada ketepatan data terma.

Ketidaktepatan profil suhu adalah disebabkan oleh pelbagai faktor termasuk penempatan sensor, ketidaktepatan peranti sensor dan hingar DSM antara-sambung. Walaupun ketidaktepatan profil suhu yang disebabkan oleh penempatan sensor dan ketidaktepatan peranti sensor telah ditangani secara meluas, kajian masih terhad dalam kesan hingar DSM antara-sambung kepada kecekapan DTM. Oleh itu, tesis ini membangunkan satu platform simulator yang komprehensif untuk menyiasat kesan hingar DSM antara-sambungan pada ketepatan data suhu dan kecekapan DTM. Hasil simulasi menunjukkan bahawa hingar DSM teruk menjejaskan data terma yang membawa kepada kemerosotan prestasi DTM yang ketara.

Untuk mengurangkan kesan hingar DSM kepada kecekapan DTM, skim toleransi kegagalan NoC yang menggunakan teknik pengiraan anggaran telah dicadangkan, dan berbanding dengan skim pengekodan standard dapat mencapai kos yang lebih rendah dari segi penggunaan kawasan dan kuasa serta meningkatkan kecekapan DTM sebanyak 38%.

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Sumber kedua kebolehpercayaan cip melibatkan penghantaran kuasa rangkaian. PDN mengalami ancaman kebolehpercayaan jangka panjang seperti pengelektrohijrahan (EM). Kehilangan pad C4 yang terhad kepada pengelektrohijrahan menyebabkan penyampaian voltan bekalan yang stabil lebih kritikal. Mekanisme kegagalan C4 lebam bergantung kepada ketumpatan arus, bunyi dan suhu voltan atas-cip. Dalam tesis ini, kami meneroka kebergantungan mekanisme kegagalan C4 lebam pada setiap nilai suhu lebam masing-masing yang boleh membawa kepada min masa untuk kegagalan (MTTF) yang lebih tepat. Hasil penyelakuan menunjukkan bahawa menggunakan suhu seragam akan meremehkan sistem MTTF sebanyak 16 kali kerana eksponensial ketergantungan kegagalan C4 lebam pada suhu.

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Declaration by Members of Supervisory Committee

This is to confirm that:

- the research and the writing of this thesis were done under our supervision;
- supervisory responsibilities as stated in the Universiti Putra Malaysia (Graduate Studies) Rules 2003 (Revision 2015-2016) are adhered to.

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LIST OF ABBREVIATIONS

C4	Controlled Collapse Chip Connection
CDF	Cumulative Distribution Function
CIBD	Crosstalk Induced Bus Delay
CV	Coefficient of Variation
DN	Deep Sub-Micron Noise
DSM	Deep Sub-Micron
DTM	Dynamic Thermal Management
DVFS	Dynamic Voltage Frequency Scaling
EM	Electro-Migration
EMI	Electro-Magnetic Interference
IP	Intellectual Property
MTTF	Mean Time To Failure
NoC	Network on Chip
PCB	Printed Circuit Board
PDN	Power Delivery Network
PN	Placement Noise
PTM	Predictive Technology Models
RO	Ring Oscillator
SN	Sensor Noise
SP_D	System Performance Degradation
UC_{ET}	Unattended Cycles in Emergency Temperature
VRM	Voltage Regulator Modules

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CHAPTER 1

INTRODUCTION

1.1 Introduction

In the previous decades, the scaling of CMOS technology enabled the semiconductor industry to successfully keep an exponential growth rate in device integration. Despite the fact that CMOS technology scaling has brought about exponentially greater transistor densities but threshold and supply voltages do not decrease sufficiently quick to avoid exponential growth in on-chip power density [12]. Figure 1.1 shows the power dissipation over multiple generations of Intel chips where each labeled point is a new chip generation and the branches are the changes in power dissipation as chips are scaled to smaller technologies.

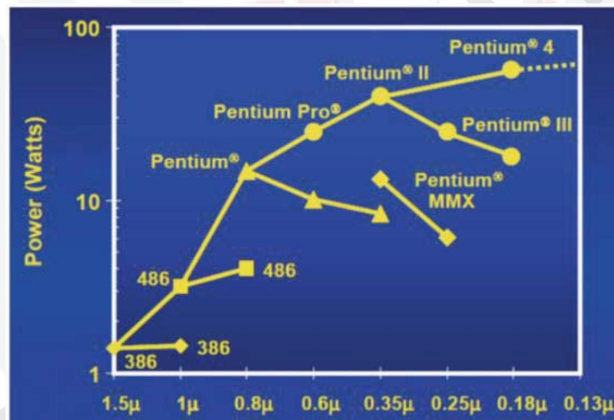

Figure 1.1: Power Dissipation Across Multiple Generations of Intel Chips [1].

Since a significant fraction of chip power consumption is converted to heat, an exponential rise in heat density is also experienced. Diverse activities and sleep modes of the functional blocks in high-performance chips cause severe hot spots on a chip, creating large temperature variations (Figure 1.2), which can decrease functionality or cause timing failure. An emergency temperature happens when temperatures increment past the maximum temperature tolerance. In emergency temperature, the chip cannot function at its required speed, resulting in erroneous computations. In addition to the risk of functional failure caused by delay increases, extended exposure to high temperatures can result in aging and electro-migration [13].

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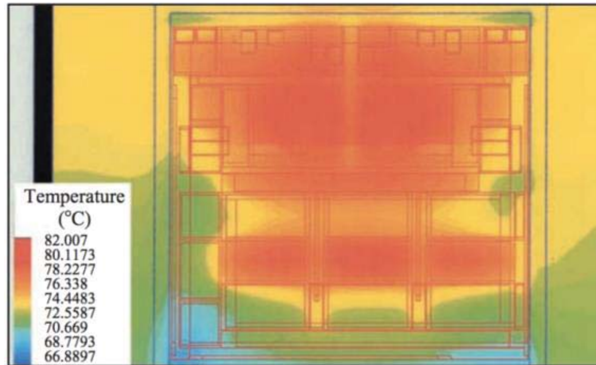

Figure 1.2: IBM POWER4 Chip Temperature Map [2]

Although temperature is one of many sources of variation facing nanoscale systems [13], its tight coupling with power dissipation and power density makes it among the most important of factors constraining nanoscale system design. In deep sub-micron, leakage current is primarily responsible for the exponential rise in heat density. The sub-threshold leakage causes the overall leakage current to increase exponentially with temperature. A positive thermal feedback may lead to a thermal runaway rendering permanent damage to the circuits. Thermal runaway is the condition where an increase in temperature causes an increase in leakage current, and the increase in leakage current dissipates enough additional power to further increase the temperature, resulting in a cycle of increasing leakage and temperature that can have unstable consequences (Figure 1.3).

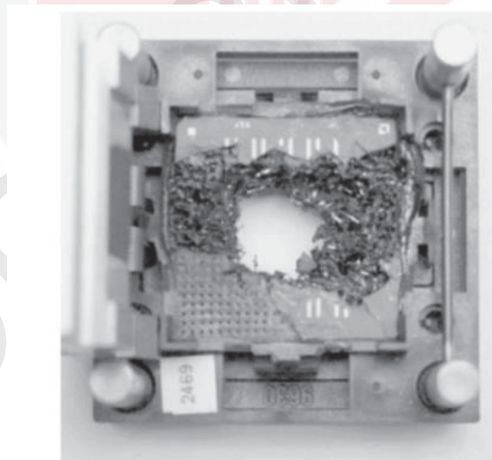

Figure 1.3: Impact of Thermal Runaway on a Test Socket [3]

Since thermal issues have been recognized as a critical barrier to utilize transistors effectively [14], it is becoming increasingly challenging to remove the massive heat generated by silicon chips. Temperature has an exponential effect on electro-migration and affects the stability of power delivery network (PDN), too.

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To maintain performance and reliability in multi-core processors, dynamic thermal management (DTM) techniques adapt the behavior of the chip based on the provided temperature profile from thermal sensors, which is transmitted using network-on-chip (NoC) in multi-core chips [15, 16, 17]. Many techniques have been proposed to manage on-chip heat dissipation [14, 4, 18]. The problems regarding the DTM and PDN reliability will be discussed in the following section.

1.2 Problem Statement

DTM efficiency is highly dependent on accurate input thermal data [14], as system performance degrades in consequence of unnecessary invokes of DTM techniques. In addition, inaccurate temperature profile lower than the actual temperature can result in late activation of DTM techniques, which could potentially result in physical damage [19]. Temperature sensing inaccuracies are cause by various factors including sensor placement, sensor device imprecision and interconnection DSM noise that will be explained in Section 2.3.3. The effect of sensor placement noise and sensor device imprecision on DTM efficiency are widely investigated [20, 21, 22, 23, 14].

One of the most worrying effects in nanometer technologies is the escalation of deep sub-micron noise. The reliability of thermal data transmitted over the bus in single core systems and over the NoC in multicore systems is challenging due to the increasing of noise in DSM technology, but to the best of our knowledge the effect of DSM noise on thermal data and consequently on DTM efficiency is missing from the literature. The above scenario motivates the need for a comprehensive investigation methodology to explore how DTM efficiency is affected by DSM noise. To highlight the dominant effect of DSM noise, this work compares the effect of DSM noise with the other noise sources affecting thermal data.

To mitigate the DSM noise impact to DTM efficiency, a specific fault tolerance scheme is proposed, exploiting inherent characteristics of DSM noise impacting the thermal data, based on approximate computing, which improve the DTM efficiency while consuming less power and area. This scheme enables continued operation of dynamic thermal management even in the presence of high ratio of DSM noise in deep sub-micron technology.

Reliability of thermal data is very important for DTM efficiency and consequently for the whole system performance and reliability. The other serious reliability challenge is a stable power delivery network to deliver sufficient current to switching transistors. Supply voltage can become noisy (i.e. drop or fluctuate) due to the PDN's intrinsic resistance, capacitance and inductance and cause timing errors and threatening program correctness. PDN suffers from long-term reliability threats such as electro-migration (EM). Temperature has an exponential effect on electro-migration and affects chip life time and voltage stability. The effect of temperature on reliability of C4 bumps are widely investigated, but a uniform temperature for the whole chip was considered. As another contribution of this study, the C4 bumps failure mechanisms dependency on accurate chip temperature is explored. This helps to reduce packaging cost and support

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more off-chip I/O channels in current and near-future technology nodes by enabling the designers provision bump allocation under different thermal maps.

1.3 Aim and Objective

The aim of this thesis is to provide a reliable thermal data transmission over NoC to maintain high DTM efficiency and investigate the reliability of power delivery network. To achieve this goal, the thesis objectives are based on three main approaches:

- Develop a simulation model to investigate the DTM performance under the effect of different sources of noise, including sensor noise, placement noise, and DSM noise, individually and in combination at 90nm technology scaling down to 22nm.
- Design and develop a specific fault tolerance coding scheme exploiting inherent characteristics of DSM noise impacting the thermal data, based on approximate computing technique.
- Develop Monte Carlo Simulation (MCS) to analyze the impact of temperature on mechanism of multiple, EM-induced, random power-C4 bump failures.

1.4 Contributions

The main contribution of this study is to investigate the impact of interconnect DSM noise on DTM efficiency and proposing a novel NoC fault tolerance scheme to mitigate the impact of interconnect DSM noise on DTM. Meanwhile, this study investigate the effect of temperature on power delivery network reliability.

1.5 Scope

The scope of this study is limited to exploiting one DTM technique to investigate the effect of all sources of noise on multicore processors. In this study the raw thermal data captured directly from sensors are used and no processing applied to them. Also in this thesis the focus is on the on-chip PDN and not the I/O bumps.

1.6 Thesis Organization

Next chapter, Chapter 2 is divided into seven sections, which introduce the required background and construct the foundation for the contributions of this thesis. Chapter 3 explains the simulation scenarios. The first simulation model is used to investigate the effect of each source of noise on thermal data and DTM efficiency. A novel approach is proposed for modeling different sources of noise and their scaling trends from 90nm to 22nm technology node. A novel fault tolerance design is also proposed due to the inherent characteristics of thermal monitoring data by exploiting approximate computing technique.

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Since the DSM noise is increasing significantly by technology scaling, it is expected that by providing specific fault tolerance scheme more power and area savings are possible while maintaining DTM efficiency in current and near future technology nodes. This chapter also introduces the performance and cost metrics used to evaluate the DTM efficiency. For the other contribution of this study, a statistical simulation model is built to analyze the mechanism and consequences of multiple EM-induced C4 pad failures under the effect of C4 pad temperature. Chapter 4 first evaluates the effect of each source of noise on thermal data and DTM efficiency individually and in combination, using the noise models and metrics presented in Chapter 3. The second part of chapter 4 compares the proposed fault tolerance scheme with the benchmark scheme in terms of hardware implementation area and power consumption, the network performance such as reliability and maximum latency and the DTM efficiency. The third part of chapter 4 evaluates the effect of C4 bump temperature on PDN reliability. The last chapter, Chapter 5, ends the thesis with some conclusion and possible future works.

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