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STANDARD CELL LIBRARY EVALUATION AND OPTIMIZATION FOR NEAR-THRESHOLD VOLTAGE OPERATION

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By

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Faculty : Engineering

Near-threshold voltage (NTV) operation digital integrated circuits have come into sight in recent decades due to the need for energy-efficient design for battery-powered devices. While earning the energy benefits from the NTV operation, the challenges of the performance degradation and variability are preventing the NTV design to be widely implemented in most computing applications. Improving energy efficiency while maintaining performance becomes the primary goal for the NTV design. The standard cell library optimization should be carefully considered to achieve better energy, performance, and area of the design. This dissertation presents the joint optimization techniques of standard cell height tuning with two different transistor layout structures, namely full diffusion (FD) layout structure and inverse narrow width effect (INWE)-aware layout structure. An increased number of optimization parameters and techniques affect the evaluation efficiency of the standard cell library at the circuit level. The evaluation efficiency (i.e., synthesis runtime) requires to be improved using the modeling technique to fasten the time-consuming process while maintaining the accuracy. An area-efficiency curve modeling framework has been proposed in this dissertation to reduce the runtime to generate the area-delay tradeoff curve for the standard cell library evaluation.

The tuning of standard cell height with FD layout structure results in 5.5% higher performance when using a taller cell height (i.e., 14-track) library, and 55.4% lower energy when using a shorter cell height (i.e., 7-track) library. As compared to the FD layout structure, the INWE-aware layout structure shows higher energy-delay improvement due to the INWE that reduces the threshold voltage when using a narrow width transistor. Two INWE-aware layout structures, namely multiplier and multi-finger, have also been explored in this study. The proposed reduced height (i.e., 6-track) library with multi-finger layout structure results in 16% performance improvement and 14% area improvement as compared to the 8-track multiplier library. Lastly, the proposed area-efficiency curve modeling framework can reduce about 16.5X to 18.5X of synthesis runtime with around 2.74% to 5.27% error from the uniform interval curve generation method.

In conclusion, the optimal NTV-operated standard cell library in terms of energy, performance, and area can be achieved by using the lower track height multi-finger layout structure as compared to FD and multiplier layout structure. Besides, the evaluation of the standard cell library on area-performance tradeoff can be sped up through the proposed area-efficiency curve modeling framework.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
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PENILAIAN AND PENGOPTIMUMAN PERPUSTAKAAN SEL STANDARD UNTUK OPERASI VOLTAN DEKAT-AMBANG

Oleh

LIM YANG WEI

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Litar bersepadu digital yang beroperasi dengan voltan dekat ambang (NTV) telah bermuncul sejak beberapa dekad kebelakangan ini kerana reka bentuk yang cekap tenaga diperlukan dalam peranti berkuasa bateri. Walaupun manfaat tenaga dapat diperolehi daripada operasi NTV, cabaran kemerosotan prestasi dan kebolehubahan menghalang reka bentuk NTV dilaksanakan secara meluas dalam kebanyakan aplikasi pengkomputeran. Peningkatan kecekapan tenaga sambil mengekalkan prestasi telah menjadi matlamat utama untuk reka bentuk NTV. Pengoptimuman perpustakaan sel standard harus dipertimbangkan dengan teliti untuk mencapai tenaga, prestasi, dan kawasan reka bentuk yang lebih baik. Disertasi ini membentangkan teknik pengoptimuman penalaan ketinggian sel standard bersama dengan dua struktur susun atur transistor yang berbeza, iaitu struktur susun atur difusi penuh (FD) dan struktur susun atur kesan lebar sempit songsang (INWE). Peningkatan bilangan parameter dan teknik pengoptimuman akan mempengaruhi kecekapan penilaian perpustakaan sel standard pada peringkat litar. Kecekapan penilaian (iaitu masa sintesis) perlu dipertingkatkan dengan menggunakan teknik pemodelan untuk mempercepatkan proses yang memakan masa dan mengekalkan ketepatan penilaian pada masa yang sama. Rangka kerja pemodelan keluk kecekapan-kawasan telah dicadangkan dalam disertasi ini untuk mengurangkan masa jalan dalam menjanakan keluk keseimbangan kawasan-lengah untuk penilaian perpustakaan sel standard.

Penalaan ketinggian sel standard dengan struktur susun atur FD telah menghasilkan prestasi 5.5% lebih tinggi apabila menggunakan ketinggian sel yang lebih tinggi (iaitu 14-trek), dan tenaga 55.4% lebih rendah apabila menggunakan ketinggian sel yang lebih pendek (iaitu 7-trek). Berbanding dengan struktur susun atur FD, struktur susun atur INWE menunjukkan peningkatan tenaga-lengah yang lebih tinggi disebabkan oleh INWE yang mengurangkan voltan ambang apabila menggunakan transistor lebar yang sempit. Dua struktur susun atur INWE, iaitu pengganda dan berbilang jari, juga telah diterokai dalam kajian ini. Perpustakaan cadangan yang mengurangkan ketinggian (iaitu 6-trek) dengan struktur susun atur berbilang jari telah menghasilkan peningkatan prestasi 16% dan pengurangan kawasan 14% berbanding dengan perpustakaan pengganda 8-trek. Akhir sekali, rangka kerja pemodelan keluk kecekapan-kawasan dapat mengurangkan 16.5X hingga 18.5X masa sintesis dan 2.74% hingga 5.27% ralat berbanding dengan kaedah penjanaan keluk yang menggunakan selang seragam.

Kesimpulannya, pengoptiuman perpustakaan sel standard yang beroperasi dengan NTV dari segi tenaga, prestasi, dan kawasan boleh dicapai dengan menggunakan ketinggian trek yang lebih rendah dan struktur susun atur berbilang jari berbanding dengan struktur susun atur FD dan susun atur pengganda. Di samping itu, penilaian perpustakaan sel standard dalam keseimbangan kawasan-prestasi boleh depercepatkan melalui rangka kerja pemodelan keluk kecekapan-kawasan yang dicadangkan.

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Declaration by Members of Supervisory Committee

This is to confirm that:

- the research and the writing of this thesis were done under our supervision;
- supervisory responsibilities as stated in the Universiti Putra Malaysia (Graduate Studies) Rules 2003 (Revision 2015-2016) are adhered to.

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LIST OF ABBREVIATIONS

AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
DFF	D Flip-Flop
DIBL	Drain-Induced Barrier Lowering
DRC	Design Rules Check
EDA	Electronic Design Automation
EDP	Energy-Delay Product
ED^2	Energy-$Delay^2$
FBB	Forward Body Biasing
FD	Full Diffusion
FF	Fast-Fast Corner
FO4	Fan-out of 4
FPGA	Field Programmable Gate Arrays
GPIO	General Purpose Input/Output
HVT	High Threshold Voltage
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit
INWE	Inverse Narrow Width Effect
I/O	Input/Output
IoT	Internet-of-Things
IR Drop	Voltage Drop

LOCOS	Local Oxidation of Silicon
LOD	Length of Oxide Diffusion
LVS	Layout Versus Schematic
LVT	Low Threshold Voltage
MAPE	Mean Absolute Percentage Error
MEP	Minimum Energy Point
MF	Multi-finger
MH	Multi-row Height
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MP	Multiplier
MW	Monolithic Width
nFD	Non-Full Diffusion
NMOS	N-channel Metal-Oxide-Semiconductor
NTV	Near-Threshold Voltage
Parasitic RC	Parasitic Resistance and Capacitance
PD^2	Power-Delay^2
PDN	Pull-Down Network
PDP	Power-Delay Product
PEX	Parasitic Extraction
PMOS	P-channel Metal-Oxide-Semiconductor
P/N Ratio	PMOS-to-NMOS Ratio
PPA	Power, Performance, and Area
PTS	Parallel-Transistor-Stacking
PUN	Pull-Up Network
RAM	Random Access Memory
RBB	Reverse Body Biasing

RC delay model	Resistor-capacitor delay model
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RSCE	Reverse Short Channel Effect
RTL	Register Transfer Level
RVT	Regular Threshold Voltage
SCE	Short Channel Effect
SDS	Single Device Sizing
SH	Single-row Height
SNM	Static Noise Margin
SoC	System on Chip
SRAM	Static Random Access Memory
SS	Slow-Slow Corner
STI	Shallow Trench Isolation
STV	Sub-Threshold Voltage
T*n*	Track-*n*
TT	Typical-typical Corner
UART	Universal Asynchronous Receiver-Transceiver
VHDL	VHSIC Hardware Description Language
VLSI	Very Large-Scale Integration
^oC	degree Celsius

CHAPTER 1

INTRODUCTION

1.1 Background

Over the decades, the exponentially increased transistor density in the integrated circuits (IC) due to the Complementary-Metal-Oxide-Semiconductor (CMOS) technology scaling has allowed more functionalities to be compacted in a single chip and become a system-on-chip (SoC) [1]. The increasing complexity in the SoC enables the standard cell-based design approach to fasten the time-to-market of the product, where the standard cells are the pre-design logic gates that able to be reusable for different circuit block design [2]. The collection of the standard cells in a library form can be optimally designed for different SoC requirements such as high-performance, low power, or smaller area.

The appearing of multi-functional SoC also leads to the diversification of semiconductor applications into different market segments such as healthcare, agriculture, automotive, communication, and consumer electronics. The diversity of applications shifted the primary design concern of integrated circuits from the speed and area to the power and energy consumption due to the different requirement needs. For instance, the battery-operated devices that are used for Internet-of-Things (IoT), wearables, and biomedical sensors require a limited energy budget to sustain the battery operating lifetime [3]. Even the high-performance computation servers used in data centers require limited power usage due to high operational costs [4].

Focusing on power or energy minimization in the design does not imply that the design performance should be ignored. The appropriated optimization should either minimize the energy consumption for a given timing requirement or maximize the performance within an energy budget [5]. This energy-performance relationship has arisen numerous research on the optimization techniques across various layers of design abstraction, from the device and circuit to the micro-architecture level. Several common optimization techniques include transistor sizing [6], [7], gate sizing [5], [8], supply voltage scaling [5], [9], threshold voltage tuning [5], [10], body biasing [11], pipelining and parallelism [9], power-gating [12], and clock-gating [12]. Jointly implementation of the techniques across the layers could achieve the global optimal solution. However, careful consideration is needed to avoid redundant area overhead and/or performance degradation.

Among the existing optimization techniques, supply voltage scaling is a well-known technique for improving the energy efficiency of the circuit due to the quadratic and linear dependency of supply voltage on the dynamic and leakage energy respectively [5], [14], [15]. One of the reasons that the energy consumption is reduced with the technology node scaling is because of the scaling of supply voltage. However, the supply voltage has almost remained constant around 65nm node and no longer delivers significant energy gains as shown in Figure 1.1 [13]. This is because substantially voltage downscaling exacerbates the performance degradation [14], [16].

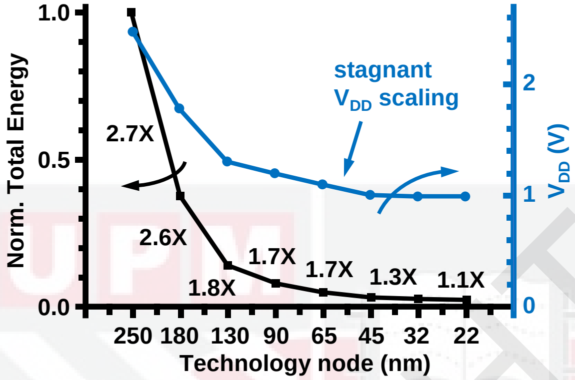

Figure 1.1 : Energy consumption reduction and supply voltage scaling over the process technology scaling. (Reproduced from [13]).

Nevertheless, the ultra-low voltage design approach has come into sight in recent years due to the acceptable range of performance from a hundred kHz to a few MHz designs in the IoT and biomedical applications [17]. The supply voltage is aggressively scaled from the nominal voltage down to the near-threshold (NTV) and sub-threshold (STV) voltages for the ultra-low voltage approach. Figure 1.2 illustrates the magnitude of energy reduction and delay degradation in a wide voltage scaling range. As the voltage scales down to the STV, the increase of leakage energy due to the increase of circuit delay eventually dominates the dynamic energy and results in a minimum energy point (MEP) as seen in the figure. Though the MEP is located in the STV region, many applications could not support this voltage range due to the exponential decrease in the circuit performance. As compared to STV operation, NTV operation sacrifices some of the energy savings with relatively higher performance. The performance gain in the NTV significantly expands the application space from the STV operation [17], [18].

Despite that the STV/NTV designs have been well explored in academic research, still, it is not common in the industry area [19]. Two major challenges that affect the robust operation in the ultra-low voltage regions are performance degradation and process variability. These forces the changes of the design techniques on the architecture, circuit, as well as standard cell library [3], [13], [14], [17], [19]–[25]. Because of the contradiction of energy and speed of the circuit, the optimization of both energy and performance is difficult to be delivered at the same time. The energy-performance optimization in the STV/NTV designs should be minimizing the energy via voltage scaling while pushing the speed through other design techniques. To proliferate the ultra-low voltage design approach for energy-efficient design, more efforts are required to improve the performance and robustness of the circuit to achieve a certain application need.

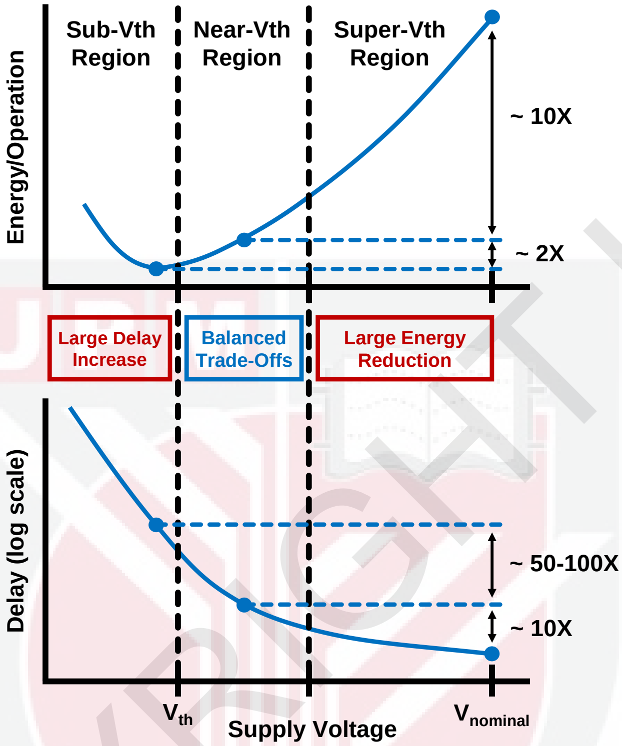

Figure 1.2 : Circuit energy and delay over a wide voltage scaling range. (Reproduce from [17]).

1.2 Problem Statement

In the past, digital integrated circuit designs in a fully custom manner potentially maximize the performance with high density and low power characteristics. However, the increased complexity of the chip that requires deliberate design for stringent performance targets takes a huge amount of human and time effort [26]. In the modern digital IC design, the standard cell-based design approach has been introduced as the key matter to meet time-to-market requirements. With the aid of the electronic design automation (EDA) tool, the IC can be constructed by a group of pre-designed and characterized logic gates, which are known as standard cells. These standard cells with different logic functions and drive strengths are usually provided by the silicon foundry or created in-house. The collection of the standard cells in a group is called standard cell library, and they can be designed and optimized to meet different power, performance, area (PPA) design targets.

Most of the currently available digital standard cell libraries in the market are well optimized for super-threshold voltage operation [22], [25]. Because of the different transistor current characteristics in the STV/NTV region as compared to the super-threshold voltage region [14], [16], [17], the existing standard cell libraries are not optimal in terms of PPA when operating at ultra-low voltage region. Therefore, optimization of standard cell libraries that operates at STV/NTV regions is highly desirable for energy-efficient digital circuits.

To address the performance degradation issue in STV/NTV design, the transistors in the standard cell need to be carefully resized [27]–[29]. Minimum transistor sizes that result in the minimum energy could worsen the delay variability and deteriorate the robustness of standard cell [30]; while the transistor sizes that ensure the reliability of standard cell is impractically large [14]. Joint design techniques with transistor sizing should be considered for ultra-low voltage standard cell design to have robust operation and better PPA optimization. In the super-threshold voltage standard cell design, cell height is one of the important parameters that are used to address the different PPA targets of the circuits. Taller height cells provide larger current drives but with larger area and power consumption; In contrast, shorter height cells result in relatively lower power and area with weaker drive strength [31]–[33]. However, the cell height parameter does not take much attention from the researcher that works on STV/NTV design.

Since the transistor drive current is exponentially dependent on the threshold voltage in the STV/NTV region, the device parasitic effect such as inverse narrow width effect (INWE) and reverse short channel effect (RSCE) now shows a significant impact on the transistor’s delay [22]. In contrast to the traditional method, the transistor sizing with INWE and RSCE consideration could lead to higher current drive, and thus, faster performance. However, the effectiveness of the INWE and RSCE are depends on the process and might cause the increase of leakage current and area. The proposed INWE-aware transistor implementation for ultra-low voltage operation in [22] can realize in either multi-finger or multiplier layout structure. Although the transistor sizes are the same for both layout structures, they exhibit different energy-delay results [34]. However, the previous works’ exploration on the INWE-aware layout structures comparison only evaluated on the inverter cell using the ring oscillator circuit, which does not present the results of the other complex circuit blocks that contain different cell functions. Again, the impact of standard cell height on energy and performance has not been studied in the previous research.

For the standard cell libraries evaluation within the context of the circuit blocks, the exploration of the energy (or area) performance tradeoff of a certain tuning parameter can be observed through the energy efficiency curve. The energy/area efficiency curve, which sometimes is known as the energy/area-delay tradeoff curve [35] or Pareto optimal curve [36], is the optimal energy/area-delay boundary corresponding to the specific parameter(s) tuning in the energy/area-delay design space. To obtain the energy efficiency curve in the standard cell-based design approach, multiple synthesis runs are required to result in various energy/area-delay solutions. The number of synthesis runs is depended on the energy/area-delay range target, and the prior study in [37] performed about 25-30 synthesis runs to obtain an energy (and area) efficiency curve. For the impractically large circuits, it might take a few hours to days in performing the multiple synthesis runs [38]. The evaluation of multiple standard cell tuning parameters (i.e., supply voltage, INWE-aware layout, and standard cell height) in ultra-low voltage design even increases the number of syntheses runs. This causes the standard cell libraries evaluation by using the energy/area efficiency curve to become more tedious and time-consuming. Therefore, a fast estimation or modeling of the energy/area efficiency curve is required for libraries evaluation.

1.3 Aim and Objectives

The main aim of this research is to propose energy-performance-area optimized standard cell libraries for near-threshold voltage operation. The following objectives are set to support the aim:

1. To develop an area-efficiency curve modeling framework for analyzing and evaluating the area-performance tradeoff of the standard cell libraries at the circuit block level.
2. To develop standard cell library using the joint techniques of transistor sizing with full diffusion layout structure and cell height tuning in optimizing the energy and performance.
3. To develop the INWE-aware layout structure with reduced cell height for energy-efficient standard cell library.

1.4 Thesis Scope

The optimization of a digital integrated circuit can be performed over different layers of design abstraction from device, circuit to micro-architecture as aforementioned. The scope of this thesis focuses on the standard cell library optimization and evaluation since the standard cells are the fundamental building blocks of the digital integrated circuit. The standard cell library optimizations mainly focus on the NTV operation to achieve better energy efficiency than requires by the battery-powered applications, such as IoT sensors, wearable, and biomedical devices. NTV operation not only benefits from the energy saving, but it also has relatively higher performance as compared to STV operation. Generally, the optimization of digital integrated circuits targets the PPA. However, energy consumption is being considered in this study instead of power, where energy is the derivation of the power and performance.

Multiple EDA tools were employed to develop the standard cell libraries as well as the implementation of Application Specific Integrated Circuit (ASIC) for the evaluation of libraries. During the standard cell libraries development, *Cadence Virtuoso* was used for schematic and layout custom design, *Mentor Calibre* was used for physical verification, *Synopsys Hspice* was used for functional verification, and *Synopsys Liberty NCX* was used for standard cell characterization. Whereas during the ASIC implementation, *Synopsys VCS* was used for register transfer level (RTL) and gate-level simulation, *Synopsys Design Compiler* was used for RTL synthesis and optimization, *Synopsys IC Compiler* was used for place and route, *Synopsys PrimeTime* was used for timing closure signoff, and *Mentor Calibre* was used for physical verification signoff.

In this study, several ASIC benchmark circuits with different functions and various number of gates, ranging from 400 to 200,000 gates were used to evaluate the developed standard cell libraries. Those circuits include the 32-bit Brent-Kung adder [39], AMBA AHB controller [40], Synopsys DW8051 processor core [41], ARM Cortex-M0 processor core [42], and AES-256 encryption core [43]. The data path block, 32-bits Brent-Kung adder is self-developed based on the Brent Kung adder architecture [39], while the AMBA AHB controller is an open-source bus controller block obtained from the ARM Design Start website [40]. Both 8-bits DW8051 and 32-bits Cortex-M0 processor cores are proprietary circuits owned by the Synopsys and ARM respectively. Since they are proprietary circuits, the Verilog RTL for both processors are encrypted and unable to viewed by the designer. Although the RTL could not be viewed, the implementation of synthesis, place and route still can be performed using the EDA tools. The AES-256 encryption core benchmark is taken from the OpenCores website [43]. For the modeling of the area-efficiency curve, the benchmark circuits from ISCAS'89 [44], which contain both combinational and sequential cells, were employed.

The CMOS process technologies that employed for the standard cell library design and evaluation throughout the thesis were different. Three existing commercial standard cell libraries which developed in TSMC 65nm process were used for evaluating the proposed area-efficient curve modeling framework because these libraries were commonly used by the industry design and academic research. Whereas the NTV standard cell library development with FD layout structure and INWE-aware layout structure were implemented in Silterra 110nm and 130nm process respectively due to the limited access to the leading process design kit (i.e., 65mn and beyond) and the chip tape-out requirement that based on the research grant funding.

Since the NTV for Silterra 110nm and 130nm process is ranging from 0.4V to 0.6V, any supply voltage value within this range can be used for the NTV design operation. However, 0.6V was applied for the standard cell library with the FD layout structure to fulfill the timing requirement of the DW8051 design. Whereas 0.4V was applied for the standard cell library with INWE-aware layout structure due to the effect of INWE to the device current is much larger at 0.4V as compared to 0.6V.

1.5 Thesis Organization

This section provides an overview of the thesis structure.

Chapter 1 briefly introduces the background of research on the ultra-low voltage design approach, problem statement, and the aim of the research.

Chapter 2 presents the literature review on the state-of-the-art research. The details of STV and NTV design techniques and challenges are also discussed. Besides, the related works to the standard cell library optimization in ultra-low voltage regions are presented in the same chapter.

Chapter 3 discusses the design flows of ASIC implementation and standard cell library development in this research. The discussion includes the EDA tools used, design environment setup and constraints, design-related parameters, and the benchmark circuits for evaluation.

Chapter 4 presents a modeling framework for the area-efficiency curve that use to evaluate the standard cell library at the circuit level. This chapter describes the existing area-efficiency curve generated using the commercial synthesis tool and then demonstrates the proposed framework to model the area-efficiency curve. The model framework is evaluated using multiple standard cell libraries and benchmark circuits.

Chapter 5 proposes a joint optimization technique that considers the transistor sizing and standard cell height tuning in optimizing the energy and performance for NTV operation. A transistor sizing method with layout consideration is discussed. The latter part of the chapter discusses the implementation of different standard cell height libraries incorporated with the proposed transistor sizing method.

Chapter 6 explores the impact of different device layout structures that utilize INWE on energy, performance, and area for NTV operation. This chapter also proposes a reduced cell height architecture for further energy-performance optimization. The evaluation of the proposed structure is demonstrated in cell- and block-level design.

Chapter 7 concludes the contributions of this research and ends with some recommendations of the possible future work.

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