



**UNIVERSITI PUTRA MALAYSIA**

**FAILURE ANALYSIS INVESTIGATION ON 2N7002LTI TMOS DEVICE  
DUE TO ELECTROSTATIC DISCHARGE(ESD) FAILURES**

**ABDUL HALIM ABDUL MANAF**

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ELECTROSTATIC DISCHARGE(ESD) FAILURES**

**By**

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the Degree of Master of Science in the Faculty of Engineering,  
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**Dedications:**

This thesis is dedicated to my parents;

Abdul Manaf Hj Abdul Rahman

Zawiah Hj Yaacob

and my wife;

Aniqah Hashim

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## LIST OF ABBREVIATIONS

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect transistor
TMOS	A type of MOSFET transistor, letter "T"
DMOS	"D" type structure Metal Oxide Semiconductor
VMOS	"V" type structure Metal Oxide Semiconductor
NMOS	N type Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
SCR	Silicon Cathode Rectifier
ESD	Electrostatic Discharge
EOS	Electrical Overstress
SOT23	A surface mount package with three legs
PAT	Parametric Abnormality Test
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model





SCM	Small Capacitance Method
TFM	Thermal Failure Modelling
STM	Simplified Thermal Model
BVGSS	Breakdown Voltage between Gate to Source
BVDSS	Breakdown voltage between drain to source
$V_{ds}$	Drain to source voltage
$V_{ds(on)}$	Drain to source on voltage
$V_{gs}$	Gate to source voltage
$V_{gs}$	Threshold voltage
$V_g$	Gate voltage or BVGSS
IGSS	Gate to source leakage current
IDSS	Drain to source leakage current
$I_d$	Drain current
I-V	Current versus Voltage
E-beam	Electron-beam
FALT	Failure Area Location Technique
SEM	Scanning electron microscope

ATE	Automatic test equipment
PC-AT	Personal computer, type AT
FIFO	First in first out
DOS	Disk operating system
FET	A trademark of a test machine
SiO <sub>2</sub>	Silicon dioxide
Si-SiO <sub>2</sub>	Silicon-Silicon dioxide
TEOS	Insulating oxide/ interlayer dielectric
N+	Heavily doped N type material
N-	Lightly doped N type material
P+	Heavily doped P type material
P-	Lightly doped P type material
V/cm	Volts per centimeter
Angstroms	10 <sup>-10</sup> meter
mA	miliampere, 10 <sup>-3</sup> Ampere
μA	microampere, 10 <sup>-6</sup> Ampere
nA	nanoampere, 10 <sup>-9</sup> Ampere



**pA**            **picoampere,**

**ns**            **nanosecond,**

**ms**            **milisecond,**

**pF**            **picofarad,**

**Kohms**        **Kiloohms,**

**Mohms**        **Megaohms,**



Abstract of thesis submitted to the Senate of Universiti Putra Malaysia in partial fulfilment of the requirements for the degree of Master of Science.

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DEVICE DUE TO ELECTROSTATIC DISCHARGE(ESD) FAILURES**

by

**ABDUL HALIM BIN ABDUL MANAF**

**APRIL 1998**

Chairman:

Faculty:

The common failures in the electronic devices e.g. Metal Oxide Semiconductor(MOS), and T type Metal Oxide Semiconductor Field Effect Transistor (TMOS) are due to Electrostatic Discharge(ESD) and Electrical Overseers(EOS). A review is carried out giving an account of various types of failures and failure analysis philosophies. investigation. methodology developed here, Seremban, between Gate to Source(BVGSS) Stress Test, Parametric Abnormality Test (PAT) to induce failure. It has been observed that the



2N7002LT1 TMOS device does not fail within 45 volts of positively as well as negatively biased voltage condition when applied to the gate and source of the device, during BVGSS Stress Test. On the other hand the Voltage Susceptibility Test has given a limiting voltage of 110 volts, for the device to fail. The failure of the devices have been studied using the failure analysis philosophy developed here and it is observed that the failure is due to thinning of the gate oxide layer. The detailed scanning electron microscope (SEM) study has been carried out to comment on the additional mechanics of failure. The amount thinning of the gate oxide layer in the various regions of the device has been found to be in the range of 800 to 950 Angstroms.



Abstrak tesis yang dikemukakan kepada Senat Universiti sebagai memenuhi sebahagian daripada syarat ijazah Sarjana Sains.

**KAJIAN PENGANALISAAN KEROSAKAN ALAT JENIS  
TRANSISTOR, 2N7002LT1 TMOS DISEBABKAN OLEH  
NYAHCASAN ELEKTROSTATIK(ESD)**

Oleh

**ABDUL HALIM BIN ABDUL MANAF**

**APRIL 1998**

Pengerusi:

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Kegagalan yang biasa berlaku kepada perkakasan elektronik seperti MOS, MOSFET dan TMOS adalah disebabkan oleh Nyahcas Electrostatik (ESD)

Lebihan Elektrikal (EOS)

beberapa jenis kegagalan dan falsafah analisis kegagalan. Kaedah baru analisis kegagalan telah dibangunkan sebagai sebahagian daripada kajian ini. Sebagai penggunaan kepada falsafah semasa bagi kaedah analisis kegagalan yang telah dibangunkan,

telah dipilih. Perkakasan

(BVGSS)



menghasilkan kegagalan. Pemerhatian menunjukkan bahawa perkakasan 2N7002LT1 TMOS tidak gagal pada 45 volt pada keadaan voltan positif dan juga negatif. Pada sudut yang lain,

perkakasan tersebut untuk gagal. Kegagalan perkakasan telah dikaji menggunakan falsafah analisis kegagalan yang telah dibangunkan dan pemerhatian menunjukkan bahawa kegagalan adalah disebabkan oleh penipisan pada lapisan get oksida. Penelitian lengkap mikroskop imbasan elektron (SEM)

maklumat tambahan yang terperinci mekanik kegagalan. Jumlah penipisan lapisan get oksida telah ditemui dalam julat di antara 800 ke 950 Angstroms.

## CHAPTER 1

### INTRODUCTION

Now a days customers do insist to have reliable and robust electronic products. It has been observed that the majority of failures are due to Electrostatic Discharge(ESD) scaled down to considerably, susceptible to ESD and EOS events, This in turn hampers the functionality of the subassemblies of the integrated circuit of the product. integrated circuits are due to ESD and EOS events. It is also observed that the failures in the Metal Oxide Semiconductor(MOS) prevent these failures it is necessary that one should understand, events affect the failure process.

The purpose of this investigation is to carryout a systematic study of failure investigation process. associate ESD event for study as this is easy to generate as compared to EOS event. There are many types of Metal Oxide Semiconductor(MOS) Semiconductor Field Effect Transistor(MOSFET) study a MOSFET device known as 2N7002LT1 TMOS, Seremban had been chosen. This device is being used in audio/radio frequency circuits in high-frequency inverters,





A systematic study of failure investigation process has been carried out and the details of the thesis is presented as follows:

Chapter 2,  
failures due to ESD and EOS events have been reviewed. The details about different models used by various investigators are also given. Various methods of failure analysis, tools and techniques along with remedial measures to avoid failures are also given. Finally the scope of the thesis is presented.

Chapter 3,  
Source(BVGSS) Stress Test, Parametric Abnormality Test, and Voltage Susceptibility Test, to be conducted to induce the failure in the device. The chapter also enumerates various test techniques in support of main tests along with associated instrumentation. A new type of failure analysis methodology is developed and explained in detail. It is also discussed as to how to implement the methodology of testing for a particular electronic device. The failure analysis methodology developed definitely contributes to the knowledge and understanding of the failure analysis philosophy. Finally various test procedures are described which are used in this investigation.

Chapter 4, describes the results and discussions. Altogether three types of tests are given in Chapter 3. The test are carried out to induced the failures in the samples. In other words the outcome of these tests lead to preparation of samples. Subsequently the failure analysis is carried out on the samples obtained from three different tests. Finally, Chapter 5,