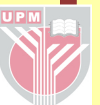
UNIVERSITI PUTRA MALAYSIA

SIMULATION AND ANALYSIS OF SHORT CHANNEL EFFECTS ON BULK AND TRI-GATE MULTIPLE INPUT FLOATING GATE MOSFET

SITI NUUR BASMIN MOHD MAAROF

FK 2008 78



SIMULATION AND ANALYSIS OF SHORT CHANNEL EFFECTS ON BULK AND TRI-GATE MULTIPLE INPUT FLOATING GATE MOSFET

By

SITI NUUR BASMIN MOHD MAAROF

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Master Of Science

July 2008

DEDICATION

This Thesis is dedicated
To

My Parents
Mohd. Maarof Abd Moksin and Nor'Aini Hassan

My Brothers and Sister
Mohd. Akmal, Siti Zatil Iman, 'Afif and Amar

Abstract of thesis prepared to the Senate of Universiti Putra Malaysia in fulfilment of the requirements for the degree of Master of Science

SIMULATION AND ANALYSIS OF SHORT CHANNEL EFFECTS ON BULK AND TRI-GATE MULTIPLE INPUT FLOATING GATE MOSFET

By

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While the scaling limits of MOSFET have been widely researched, the scaling of Multiple Input Floating Gate (MIFG) MOSFET devices has been receiving less attention. The MIFG MOSFET has short channel effect that arises from the scaling of the device at a more significant level than the typical MOSFET because the existence of the floating gate electrode widens the distance of the input gates and the channel. This distance weakens the ability of the gate to control the channel charge effectively which leads to higher short channel effects.

Tri-gate MIFG MOSFET proposed in this thesis is combination technologies of a MIFG MOSFET planar device structure and a 3-D Tri-gate transistor. The ability to circumvent short channel effect of the Tri-gate MOSFET are emphasized on the subthreshold characteristic of the device by monitoring the DIBL and subthreshold slope parameter and is compared with a bulk MIFG MOSFET structure at equal technology parameter. The device coupling capacitor and voltage bias at control gate are varied in order to analyze its influence on these effects. Two different structures, Top Tri-gate MIFG MOSFET and Side Tri-gate MIFG MOSFET were studied. This

research focuses in the physical MIFG MOSFET structures and analyzes its short channel effect behavior by performing 3-D computer-based numerical simulations using Davinci simulator.

There were two sets of results obtained when comparing the short channel effect of the two Tri-gate MIFG MOSFETs with bulk MIFG MOSFET. At $C_2/C_1 \leq 1$ and at variable V_{gate2}, Tri-gate MIFG MOSFETs shows better results than the bulk MIFG MOSFET in subthreshold slope and DIBL effect with best in $C_2/C_1 = 0.5$ followed by $C_2/C_1 = 1$. From the electrostatic potential distribution graph of the devices, the better short channel effect suppression can be interpreted as a result of better gate controllability in the Tri-gate MIFG MOSFET than the bulk MIFG MOSFET channel.

However, for $C_2/C_1 > 1$, overall Tri-gate MIFG MOSFETs shows worse short channel effects than the bulk MIFG MOSFET. The Tri-gate device structure shows the worst short channel effect behavior than the bulk device structure which contradicts with the previous results. The correlation between $C_2/C_1 \leq 1$ and $C_2/C_1 > 1$ for a two-input gates in the Tri-gate MIFG MOSFET to control short channel effects is that gate 1 as the signal gate has to have a large area in order to control the channel effectively. At the same time, the voltage applied at gate 2 has to be controlled just to be sufficiently enough to turn on the transistor. The placement of the input gates as the top and side of the floating gate does give significant effect in the simulation results where the Top Tri-gate MIFG MOSFET gives better or approximately same data with the Side Tri-gate MIFG MOSFET.

It can be concluded that the suppression of short channel effects of the Tri-gate MIFG MOSFET must not only consider the Tri-gate structure itself, but must also take into account the area of input gate coupling capacitance, voltage bias and placement of the input gates.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan Ijazah Sarjana Sains

SIMULASI DAN ANALISIS KESAN SALURAN PENDEK TERHADAP MOSFET BULK DAN MOSFET TIGA-GET PELBAGAI MASUKAN GET TERAPUNG

Oleh

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Batasan penskalaan peranti MOSFET dikaji secara meluas. Namun begitu, kajian terhadap pengecilan MOSFET Pelbagai Masukan Get Terapung (MIFG) masih mendapat kurang perhatian. Kesan saluran pendek terhadap MOSFET MIFG akibat pengecilan peranti adalah lebih tinggi jika dibandingkan dengan peranti MOSFET biasa disebabkan oleh kehadiran elektrod terapung yang melebarkan jarak di antara get masukan dan saluran. Jarak ini melemahkan kebolehan get untuk mengawal cas saluran secara berkesan yang membawa kepada kesan saluran pendek yang lebih tinggi.

MOSFET Tiga-get MIFG yang diperkenalkan di dalam tesis ini adalah integrasi teknologi struktur satah peranti MOSFET bulk MIFG dan 3-D Tiga-get. Keupayaan MOSFET Tiga-get dalam memperbaiki kesan saluran pendek memberi fokus khususnya pada ciri *subthreshold* peranti dengan melihat parameter DIBL dan kecerunan *subthresold*. Kajian ini membuat perbandingan keputusan antara MOSFET bulk MIFG dan MOSFET Tiga-get MIFG pada parameter teknologi yang

sama. Kemuatan berpasangan peranti dan aplikasi voltan pada get kawalan dipelbagaikan bagi menganalisa pengaruhnya ke atas kesan saluran pendek. Dua struktur berlainan, MOSFET Tiga-get Atas MIFG dan MOSFET Tiga-get Sisi MIFG dikaji. Kajian ini memfokuskan terhadap struktur fizikal MIFG MOSFET dan menganalisa kelakuan kesan saluran pendeknya dengan melakukan simulasi *numerical* 3-D berasaskan komputer menggunakan pensimulasi Davinci.

Terdapat dua set keputusan apabila membandingkan kesan saluran pendek bagi kedua-dua MOSFET Tiga-get MIFG dengan MOSFET bulk MIFG. Pada keadaaan $C_2/C_1 \leq 1$ dan V_{gate2} dipelbagaikan, MOSFET Tiga-get MIFG menunjukkan keputusan yang lebih baik daripada MOSFET bulk MIFG pada keputusan kecerunan s*ubthreshold* dan kesan DIBL. Keputusan yang terbaik diperolehi pada $C_2/C_1 = 0.5$ diikuti dengan $C_2/C_1 = 1$. Daripada graf taburan potensi elektrostatik peranti, keberkesanan kesan saluran pendek tertahan yang baik boleh diterjemahkan sebagai hasil keupayaan get untuk mengawal saluran di dalam MOSFET Tiga-get MIFG dengan baik berbanding MOSFET bulk MIFG.

Namun begitu, Tri-get MOSFET MIFG pada $C_2/C_1 > 1$, secara keseluruhannya menunjukkan kesan saluran pendek yang lebih buruk berbanding MOSFET bulk MIFG dimana ia bertentangan dengan keputusan sebelum ini. Hubungkait antara $C_2/C_1 \leq 1$ dan $C_2/C_1>1$ bagi kedua-dua input get di dalam Tiga-get MOSFET MIFG bagi mengawal kesan saluran pendek adalah get 1 yang bertindak sebagai get isyarat memerlukan ruang yang besar bagi mengawal saluran secara efektif. Pada masa yang sama, V_{gate2} perlu dikawal supaya ia hanya memadai untuk menghidupkan peranti. Kedudukkan input get pada atas dan sebelah get terapung memberi kesan terhadap

keputusan simulasi dimana Tiga-get Atas MOSFET MIFG memberikan keputusan yang lebih baik atau sama dengan Tiga-get Sisi MOSFET MIFG.

Kesimpulannya, pengurangan kesan saluran pendek yang baik dalam Tiga-get MOSFET MIFG tidak boleh dianalisa dengan hanya mempertimbangkan struktur fizikal Tiga-get sahaja, tetapi juga perlu mengambil kira keluasan get masukan kemuatan berpasangan, aplikasi voltan dan kedudukkan input get.

ACKNOWLEDGEMENTS

In the name of Allah, The Most Gracious and The Most Merciful.

Alhamdulillah. I would like to express my deep gratefulness to my supervisor, Dr. Roslina bt. Mohd. Sidek, for her guidance, helpful advice, generous encouragement and motivation, never-ending patience, kind attention and willingness to assists me throughout this research. I have learnt a lot of useful knowledge from her throughout this research. Thank you very much to my supervisory committee members, Prof. Dr. Sudhanshu Shekhar Jamuar, for knowledge sharing and advice. His support and assistance helped me to complete this research work till the end.

I acknowledge Universiti Putra Malaysia for carrying out helpful programs in assisting the postgraduates to achieve good quality in research and writings. I am also thankful to Farizal Muzammil b. Abd. Wahab and Wong Wei Siung of Trans-Dist Engineering Sdn. Bhd. for providing technical support. My sincere appreciation also goes to all Electrical and Electronic Engineering staffs and master and PhD students year 2004-2007, who have helped and guided me throughout my studies. Thank you to other individuals who I have not mentioned but have helped me in any possible way.

Last but not least, I would like to express heartiness gratitude and love to my parents, family and friends for their love, encouragement and support.

I certify that a Thesis Examination Committee has met on 31 July 2008 to conduct the final examination of Siti Nuur Basmin Mohd Maarof on her thesis entitled "Simulation and Analysis of Short Channel Effects on Bulk and Tri-Gate Multiple Input Floating Gate Mosfet" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

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Date: 9 July 2009

DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

____

SITI NUUR BASMIN MOHD MAAAROF

Date:

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LIST OF ABBREVIATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
*v*MOS	Neuron Metal Oxide Semiconductor
3-D	Three Dimensional
MIFG	Multiple Input Floating Gate
VLSI	Very Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
DIBL	Drain Induce Barrier Lowering
ITRS	International Technology Roadmap For Semiconductors
SOI	Silicon On Insulator
AMD	Advances Micro Devices
IBM	International Business Machines
IC	Integrated Circuit
EPROM	Erasable and Programmable read-only memories
EEPROM	Electrically Erasable and Programmable read-only memories
ETANN	Electrically Analog Trained Neural Network
FGMOS	Floating Gate Metal Oxide Semiconductor
D/A	Digital/Analog
A/D	Analog/Digital
DNA	Deoxyribonucleic acid
CDMA	Compact code division multiple access
C*v*MOS	Chemoreceptive neuron Metal Oxide Semiconductor
SCR	Silicon Controlled Rectifier
DELTA	Fully depleted lean channel transistor

BOX	Buried Oxide

CHAPTER 1

INTRODUCTION

1.1 Evolution of MOSFET

The modern metal-oxide-semiconductor-field-effect-transistor (MOSFET) was first demonstrated in 1960 at Solid State Device Research Conference [1]. This technology came into industry in 1960 with the development of a workable silicon dioxide growth on silicon. This finding to produce the insulating layer in situ on the substrate opened up the earlier works, making the concept of the MOSFET device a practical reality [1].

The MOSFET technology consistently improves over these years and continuously expands with intense research progress. In 1992, Shibata, T. and Ohmi, T. [2] introduced a unique MOSFET which they called Neuron MOS (*v*MOS) transistor due to its functional similarity to a simple neuron model. Now, *v*MOS transistor is also widely known as Multiple-Input Floating Gate MOSFET (MIFG MOSFET) [3]. MIFG MOSFET structure can be visually described as a conventional MOSFET with several input gates attached to the floating gate of the MOSFET. The electrode is known as a floating gate because no connection is in contact with it as illustrated in Figure 1.1 where two-input gates are separated by the floating gate through an oxide layer.

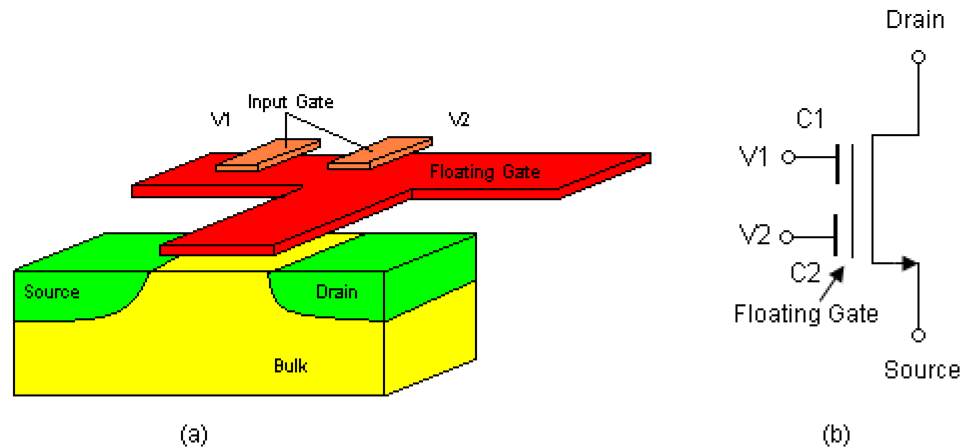

Figure 1.1: Two-input MIFG MOSFET (a) Device Structure (b) Circuit Symbol

1.2 MIFG MOSFET Contributions in VLSI Technology

MIFG MOSFET has proven to be very successful reducing the VLSI burden in carrying out intelligent circuit designs. Many researches [4, 5, and 6] have been done to expand this transistor concept technology for circuit application. Shouli, Y and Edgar S.S [7] reported that MIFG MOSFET offers an alternative solution for circuit designers to produce efficient low voltage circuits with also reduced power supply restriction via adjusting the transistor threshold voltage.

The threshold voltage seen from the input gates can be changed by varying the amount of static charge on the floating gate through ultra violet shining, hot-electron injection and Fowler-Nordheim process [7]. Other than this, the threshold voltage could also be varied by applying an external bias voltage at the input gates of the transistor. The applied voltage creates an electric potential that influences the charge to invert the silicon surface channel which then turns on the transistor. The advantage of this

technique is that it can be done after fabrication of the transistor to compensate for both manufacturing problems as well as a given operating environment. Through these programming techniques, it gives the ability for MIFG MOSFET to operate in compatible low voltage supply by lowering the threshold voltage at a desired value.

Several circuits implementing floating gates in its design have been reported to have improved area consumption while having better circuit performance when compared to the conventional MOSFET. The active resistor introduced by Popa, C [4] is described to have reduced area consumption, improved linearity and frequency response by replacing the conventional MOSFETs with MIFG MOSFETs. Ochiai, T and Hatano, H [5] had successfully designed a multiplier circuit using MIFG MOSFETs. The circuit was claimed to have layout area 60% of the conventional CMOS multiplier and with improved 15% speed performance than that for the CMOS multiplier with the same design rule. With the shrinking of VLSI circuits and denser integrated circuits, these findings are welcoming for the future technology in decreasing the minimum feature size and realizing Gordon Moore's law (that states the number of components per chip double every three years) [8].

Another interesting fact on the MIFG MOSFET is that the multiple gates available by its natural structure enable it to be used in multiple valued logic technology. Multiple Valued Logic is an interesting developing technology that has a potential advantage over binary logic which means that it can provide an increasing data processing capability per unit area with a reduced number of interconnections. The Multi-Valued Flip-Flop circuit