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FAULT TOLERANCE OF L1 DATA CACHE MEMORY INDUCED BY INTRINSIC PARAMETERS FLUCTUATION IN SUB 10nm UTB-SOI MOSFETs

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By

RABAH ABOOD AHMED

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirements for the Degree of Doctor of Philosophy

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TO MY FAMILY

Abstract of thesis presented to the Senate of University Putra Malaysia in fulfillment of the requirement for the degree of Doctor of philosophy

FAULT TOLERANCE OF L1 DATA CACHE MEMORY INDUCED BY INTRINSIC PARAMETERS FLUCTUATION IN SUB 10nm UTB-SOI MOSFETs

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February 2013

Chair: Khairulmizam Samsudin, Ph.D.

Faculty: Engineering

Currently, the development of models at higher level of abstractions (system-level) to be able to incorporate effects at lower levels of abstractions (process /transistor) is in demand. This thesis addresses issues to enabling computer system simulation model in the presence of cell failures in L1 data cache corresponding to the impact of Intrinsic Parameters Fluctuation (IPF). These time-independent transistor-level sources of variation are randomly characterized in nature. This makes it difficult for the designer to include IPF impact in the design plan to overcome. This computer model is vital to analyze and evaluate credibly the effectiveness of L1 cache fault tolerance techniques in controlling the implications of IPF cell failures on microprocessor reliability and yield.

The objectives of this thesis are (i) to devise a framework to simulate system-level environment in the presence of L1 data cache cell failures corresponding to the impact of IPF, (ii) to introduce an evaluation method for deduce the effectiveness of L1 cache fault tolerance techniques in handling the actual error pattern caused by IPF cell failures in computer system under test and workload conditions, and (iii) to investigate the implications of L1 data cache faults induced by the individual and combined impact of IPF sources on reliability of a general-purpose microprocessor.

The case study of this thesis is the impact of cell failures in the data array of L1 data cache in Intel Strong ARM@SA-1110 microprocessor. The failure models are generated corresponding to the individual and combined impact of Random Discrete Dopants in the source/drain regions (RDD), Line Edge Roughness (LER) and Body Thickness Variation (BTV) as the main sources of IPF in next nanometre-scale Ultra-Thin Body Silicon-on Isolator (UTB-SOI) transistor generations on Six-Transistors Static Random Access memory (6T SRAM) cell stability. The L1 cache fault tolerance techniques evaluated are hardware redundancy, parity check, Hamming single error correction double error detection (SECDED), and Hamming triple error detection (TED).

It was found that the rate of read faulty cells will rapidly increase in 6T SRAM cache with continued scaling of UTB-SOI device beyond 10 nm gate length. L1 cache conventional fault tolerance techniques, i.e. hardware redundancy, parity check, and SECDED, might be able to hold the implications of IPF cell failures in L1 data cache based 7.5 nm and 5 nm UTB-SOI device, particularly when 6T SRAM is designed with cell ratio of two. However, the effectiveness of these techniques was found to be sensitive to the existence of any faulty word in cache. Hence, their immunity against any transient fault that might occur during system operation will significantly degrade. Experimental results showed that in L1 data cache based on 5 nm UTB-SOI device, hybrid hardware redundancy with TED would achieve 68.2 percent of microprocessor chip yield in applications tolerate 10 percent performance loss bound. This indicates that employing these techniques in industry will assist to keep 6T SRAM cache scalability even with the increasing impact of IPF.

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Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

HAD TERIMA KEROSAKAN UNTUK MEMORI CACHE DATA L1 YANG TERARUH OLEH FLUKTUASI PARAMETER INTRINSIK DALAM UTB-SOI MOSFETs LEBIH KECIL DARIPADA 10nm

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Kini, pembangunan model pada peringkat pemisahan yang lebih tinggi (peringkat system) supaya boleh digabungkan dengan efek-efek kepada peringkat pemisahan yang lebih rendah (proses/transistor) mempunyai banyak permintaan. Banyak projek dan penyelidik menumpukan kajian mereka untuk mencapainya. Tesis ini menumpukan kepada isu-isu untuk membolehkan simulasi system computer dalam kehadiran kegagalan sel-sel cache data L1 berkaitan dengan impak dari Intrinsic Parameters Fluctuation (IPF). Sumber-sumber variasi pada peringkat transistor yang tidak bergantung kepada masa ini digambarkan secara rawak. Ini menyebabkan kesukaran bagi para pereka untuk menyingkirkan atau memasukkannya ke dalam perancangan rekabentuk untuk diatasi. Model computer ini adalah penting untuk menganalisa dan menilai dengan kredibel keberkesanan teknik had terima kegagalan cache L1 dalam mengawal implikasi-implikasi kegagalan sel IPF kepada keutuhan dan hasil mikropemproses.

Objektif-objektif tesis ini ialah; (i) untuk mereka sebuah rangka untuk mensimulasikan sekitaran peringkat system dengan kehadiran kegagalan data cache L1 berkaitan dengan impak kepada IPF, (ii) untuk memperkenalkan kaedah evaluasi untuk teknik had terima kegagalan cache L1untuk menyimpulkan keberkesanannya dalam mengendalikan corak ralat yang disebabkan oleh sel IPF yang gagal dalam system computer di bawah kondisi ujian dan bebanan kerja, (iii) untuk mengkaji implikasi-implikasi ke atas keutuhan mikropemproses serbaguna dengan cache data L1 teraruh dengan impak-impak individu dan kombinasi dari sumber-sumber Fluktuasi Parameter Intrinsik.

Kajian kes untuk tesis ini ialah impak kepada kegagalan sel dalam tatasusun data untuk cache data L1 di dalam mikropemproses Intel Strong ARM@SA-1110. Model-model kegagalan itu dijana berdasarkan kepada impak-impak individu dan kombinasi dari Random Discrete Dopants dalam kawasan sumber/susutan (RDD), Line Edge Roughness (LER) dan Body Thickness Variation (BTV) sebagai sumber utama IPF dalam skala nanometer seterusnya bagi generasi transistor (UTB-SOI) pada kestabilan sel 6T SRAM. Teknik had terima kegagalan cache L1 yang dinilai ialah lewahan perkakasan, semakan parity, SECDEC, dan TED.

Adalah didapati bahawa kadar sel pembacaan rosak akan naik dengan pantas dalam cache 6T SRAM dengan pengecilan berterusan peranti UTB-SOI melebihi panjang get 10nm. Implimentasi secara agresif teknik konvensional had terima kegagalan cache L1 iaitu lewahan perkakasan, semakan parity, dan SECDEC mungkin boleh membawa implikasi kepada kegagalan sel IPF dalam cache data LI berdasarkan 7.5nm dan 5nm peranti UTB-SOI, terutamanaya apabila 6T SRAM dicipta dengan nisbah sel dua. Walaubagaimanapun, keberkesanan teknik-teknik ini adalah sensitive kepada kehadiran apa sahaja kata yang salah dalam cache. Oleh sebab itu, keimunan mereka terhadap apa sahaja kesalahan sementara yang mungkin berlaku sewaktu operasi system akan berkurang dengan nyata sekali. Keputusan eksperimen menunjukkan bahawa cache data berdasarkan 5nm peranti UTB-SOI, kelewahan perkakasan hybrid dengan TED boleh mencapai 68.2 peratus dari mikropemproses hasil cip dalam aplikasi yang boleh menahan 10 peratus kehilangan prestasi. Ini menandakan bahawa menggunakan teknik-teknik dalam industri akan membantu untuk menyimpan 6T SRAM cache kebolehan untuk diskala walaupun dengan semakin meningkat kesan IPF.

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RABAH ABOOD AHMED

I certify that a Thesis Examination Committee has met on 7th February 2013 to conduct the final examination of Rabah Abood Ahmed on his thesis entitled "**Fault Tolerance of L1 Data Cache Memory Under the Influence of Intrinsic Parameter Fluctuation in Sub 10nm UTB-SOI MOSFETs**" in accordance with Universities and University Colleges Act 1971 and the Constitution of the University Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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DECLARATION

I declare that the thesis is my original work except for the quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at universiti Putra Malaysia or at any other institution.

RABAH ABOOD AHMED

Date: 7 February 2013

TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

β	Cell ratio
μ	Mean value
σ	Standard Deviation
efa	Effectiveness factor of area
efc	Effectiveness factor of correction
L	Number of rows in cache data array
M	ECC practical design factor
m	The number of syndrome bits
N	Number of bit cells per FTT word
N_{TR}	The number of transistors in L1-dcache data array in a wafer area
$P\ (F\_Cell)$	Probability of faulty cell in cache
P_{RC}	Probability of reliable cache
P_{Z_Sy}	Probability of the entire syndrome bits to be zero
r	Number of faulty bit cell in FTT word

CHAPTER 1

INTRODUCTION

1.1 Motivation

Semiconductor industry continues to shrink transistor dimensions for decades to gain more functions and performance, while maintaining the cost for a chip. According to Moore's Law [1], the number of components per chip doubles roughly every two years. This aggressive scaling process to the conventional device architecture such as bulk MOSFET is rapidly approaching fundamental physical limits. Short-channel effects, lack of performance, material limitations and technological difficulties are increasing challenges hindering conventional MOSFET from reaching the ultimate scale [2]. For instance, the required high-channel doping to control short-channel effects are ultimately tradeoff the device performance degradations and increase in threshold voltage variations.

In spite of high-k/metal gate technology introduction, the fabrication process of a conventional MOSFET device in nanometer dimensions (i.e. sub-10 nm physical gate length) poses difficulties in controlling device-to-device variations due to the increasing role of intrinsic parameters fluctuation (IPF). Random Discrete Dopant (RDD) [3, 4, 5, 6], Line Edge Roughness (LER) [7, 8, 9], and Oxide Thickness Variation (OTV) [10] are the most important sources of IPF in conventional MOSFET device [11]. These sources of variations are static and associated with the fundamental discreteness of charge and matter in ultra-small devices [12] and cannot be removed by strictly controlled process steps or improved fabrication equipment [13].

Due to the difficulty in characterizing all IPF sources by any design parameter(s), it is expected to change the current predictable design approaches to approximations. In particular, the impact of RDD in conventional MOSFET's channel region was already predicted to become a barrier to achieve device ultimate scale [14, 3].

For the purpose of ensuring the continuity of Moore's Law, an alternative device is required to replace the conventional bulk MOSFET. Recently, the International Technology Roadmap for Semiconductors (ITRS) [15] presented a novel MOSFET device architecture for sustaining MOSFET devices to scale deeper in nanometer regions. Ultra-Thin Body Silicon-on Insulator (UTB-SOI) MOSFET with its very low doping concentration in channel region will have inherent immunity against RDD sources of IPF, and offers a superior electrostatic integrity and better performance in comparison with the conventional MOSFET [16].

In ultra small UTB-SOI transistors, fluctuations in numbers and positions of the discrete dopant atoms in device source/drain regions have been found to be unavoidable source of IPF. Moreover, due to the fabrication process limits, LER has introduced as another source of IPF. The roughness of device line edge effectively introduces variation in each device active channel length. In addition, the inherent ±1 atomic layer roughness of the top and bottom Si/SiO_2 interfaces will also contribute in introducing the body thickness variation (BTV) variability in each individual device active channel region. The resultant of the combined effects of RDD in source/drain region, LER, and BTV will exacerbate the electrical mismatch between the similar devices [17].

It has been experimentally demonstrated at the device and circuit level that with the continued scaling of MOSFET device, IPF will adversely affect digital circuits performance and functionality [18, 13]. Particular attention has been given to investigate the impact of IPF sources on Static Random Access Memory (SRAM) functionality [19, 20].

The six-transistor (6T) SRAM is the dominant SRAM architecture used in contemporary high performance microprocessors. As the minimum size transistors are used to minimize cell area, 6T SRAM becomes the most vulnerable to manufacturing-related variations and intrinsic parameters fluctuation impacts [21]. Particularly, IPF sources are expected to have the dominant adverse impact on 6T SRAM cell stability in comparison with other manufacturing-related variations [22]: Increasing the impact of IPF sources exacerbates the electrical mismatch between the neighboring transistors in cell. This mismatch would degrade cell stability and might cause cell failure. Consequently, a catastrophic number of cache cells are expected to become faulty.

The implications of IPF cell failures is expected to adversely affect the reliability of the corresponding 6T SRAM cache memories and eventually will affect microprocessor chip yield. This would enforces cache system designers to go beyond design plan to the post-silicon phase to ensure cache system dependability (i.e reliability, error correction , and error detection). Modern processors have large specialized and multi-level cache memory; however, particular attention have been given toward L1 data cache as the most susceptible component to the impacts of IPF sources in cache memory system [23, 24].

As the process and technology to build the next generation devices and IC are very complex and still unavailable, several simulation methodology at circuit-level have been introduced to investigate the implications of IPF cell failures on 6T SRAM cache yield [25, 26, 13]. Approaches of circuit-level simulation are limited because it is only suitable to investigate a small part of the systems associated with a circuit block. Moreover, evaluation of IPF cell failures on cache chip yield must consider cache fault tolerance techniques in handling these failures - with accepted area and performance overhead. At circuit level, the evaluation process either depend on an outdated guidelines [27] that does not consider recent cache fault tolerance techniques, or they consider only the hardware side of the system without considering the interactions with software [28]. Adopting only one of these evaluations might not lead to the optimal design decision that could be very expensive in cost and time.

It is critically important to examine the implications of intrinsic parameter fluctuation at system-level - to understand and evaluate clearly the ability of system level techniques in handling the incurred failures [29]. Mainly, two methods have been used to model the implications of cache cell failures to system-level simulations. The first method is by modeling the physical presence of cell failures (failure model) in cache system [30, 31]. Although, this methodology evaluates based on system-level fault tolerance techniques, the yield evaluation process can be considered as an extension to that used by circuit-level approaches; since it only considers the probability of producing a cache chip with safe failures : tolerance techniques that can guarantee to handle all the failures. In case of evaluating a cache fault tolerance techniques with the capability of handling a limited ratio of unsafe failures, this method will be unable to capture the tolerance capability of these techniques.

For the second method, the faults incurred due to these failures (fault model) are used to evaluate the effectiveness of the tolerance techniques in handling the failures. The evaluation of this method depends on how this fault model is represented. One general approach is performed by integrating a pre-prepared fault models that was previously proven to be a representative for the general pattern of fault occurrence in system [32]. This approach is not credible to modeling the implications of IPF cell failures, since it did not represent the actual fault pattern incurred in a system under test and workload conditions. A credible IPF fault model requires to comprehensively capture system workload interactions with fault mechanism of each faulty cell in cache introduced by IPF.

In the near future, a decision to adopting UTB-SOI technology for scaling 6T SRAM cache memory to nanometer regime requires to take in consideration the effects of the increasing rate of cell failures in cache induced IPF sources. Thus, there is an urgent need for a computer-aided design tool capable to credibly evaluate the effectiveness of cache cell failure tolerance techniques to controlling the implications of this problem on cache reliability, and the tradeoff that imposed by these techniques on performance. Devise such a tool will be vital to enabling system designers and manufacturers to taking the optimal decision which save lot of efforts, time and money. Furthermore, this tool will help to accelerate the development process of fault tolerance techniques.

1.2 Aim and Objectives

The major aim of this thesis is to investigate the system-level implications of 6T SRAM cell failures in L1 data cache induced by different sources of intrinsic parameter fluctuation in nanometer scale UTB-SOI on the general-purpose microprocessor reliability and yield. Therefore, the objectives of this thesis are:

1. Devise a framework to simulate system-level environment with 6T SRAM data array failures in L1 data cache corresponding to the impact of intrinsic parameters fluctuation.

2. Propose an evaluation method to L1 cache fault tolerance techniques to handle cell failures introduced by intrinsic parameters fluctuation.

3. Investigate the implications of L1 data cache faults induced by the

individual and combined impact of intrinsic parameter fluctuation sources in 10 nm, 7.5 nm, and 5 nm gate lengths UTB-SOI device on reliability and yield of a general-purpose microprocessor.

For the first objective, a framework was developed using virtual computer platform capable to simulate a computer system operation in the presence of IPF cell failure pattern in 6T SRAM L1 data cache memory. SIMICS [33], the full system simulator, is used to simulate this computer platform. By default, SIMICS as the instruction set simulator, does not provide the mechanism to inject the effects of device and circuit levels into the simulated computer platform. This led to an integral strategy built in the SIMICS environment accounts for the impact of IPF sources in the simulated platform. The extraction of the impacts of IPF sources on 6T SRAM cache is performed by adopting the experimental results from a prior circuit-level simulation work. These results are statically processed and modeled as a virtual chip that represents the failure models induced by IPF sources. This framework enabled the capturing of the interactions between IPF cell failures model and its implications on system reliability and performance. The credibility of modeling these implications is also related with system workload. Therefore, a set of general-purpose benchmarks is applied on the virtual computer platform to simulate workload of the general-purpose applications.

The most important results that this framework must provide is from evaluating the effectiveness of fault tolerance techniques to control the implications of IPF failures on cache reliability and yield. Conventional methods to evaluate L1 cache fault tolerance techniques do not take into account the failures interactions with system software layer, This could lead to a pessimistic perception, where the likely and unlikely effects will take the same occurrence probability. More pragmatic perceptions can be obtained by generating cell failures model based on the functional characteristics of the vulnerable 6T SRAM that captures IPF impacts at the lower level of abstraction (transistor-level). The derived faults will then be propagate up through system-level. Therefore, the second objective led to the introduction of a methodology specifically tailored to capture the effectiveness of L1 cache fault tolerance techniques which includes the software operation nature. Based on this methodology, fault tolerance techniques often used at L1 cache are modeled in the framework in such a way that can be introduced individually or in hybrid. These models provide statistics aggregated during system operation that helps to demonstrate in detail the ability of these techniques to maintain the reliability of the system and the imposed sacrifices in performance. This developed framework became a tool to estimate the margin of IPF sources impacts in nano-scale UTB-SOI device on system reliability and yield. Moreover, the reproducible experiments used in this methodology can assist the designer and developer of the fault tolerance techniques to understand in detail their effectiveness limits, which helps to develop these techniques faster.

In the proposed framework for evaluating fault tolerance mechanisms in the cache, there is a third objective which is investigating the implications of different sources of IPF in next generation UTB-SOI MOSFETs with channel lengths from 10 to 5 nm on the reliability and performance of the system. Particularly, the concentration on L1 data cache which is considered as the most sensitive component in computer architecture to the sources of variations [23, 31]. The study of each source of IPF in UTB-SOI is critically important to help the researchers community to focus their efforts towards the most aggressive sources. Moreover, the comprehensive investigation of the combined impact of all IPF sources, since their impacts are simultaneous in 6T SRAM cell, will lead to understanding exactly the extent of the impact of this process-level phenomenon.

1.3 Scope of the Study

- This research only consider RDD, LER, BTV sources of IPF in (10, 7.5, and 5) nm gate length UTB SOI in room temperature conditions, and exclude any other intra or inter die source of variations.

- It is only considered the impact of IPF on 6T SRAM stability and its related failures (read, and write) in the data portion of the L1 data cache of general purpose microprocessor.

- The occurrence of soft error or dynamic error in cache during system operation has been excluded.

- This investigation does not take into account the extra circuitry to implement the tolerance techniques.

1.4 Thesis Contributions

This study has introduced many key contributions to the state of the art in computer system modeling and validation techniques. The main contributions are listed as follows:

- A technique to incorporate information of cell failure model induced by IPF sources into system-level simulator as a lookup file to describe in detail the position and type of each failure in cache data array. Although in this study the focus is towards cache data array, using this technique can be expanded to include other cache portions using 6T-SRAM array such as cache tag array, fault tolerance parity bits array, etc. Empirically, this technique has been found to be capable to characterize accurately IPF cell failure model to system-level simulator by keeping the LUPF size relatively small. This small size LUPF is enabled to fit inside the memory of the host machine that reduces the effects on system simulation speed.

- A scheme to inject the actual error pattern induced by cache cell failures dynamically into system-level environment. This scheme deduces error pattern via the fault mechanism of each failure and its interaction with real system workload. This fault injection scheme provides two simulation mode that help to analyze the implications of cell failures on cache fault tolerance. The normal mode invokes fault mechanisms and propagates the error(s) through cache transactions up to the system-level environment. Fault emulation mode would just emulate faults by invoking the handler of fault mechanisms without enabling the error injection into system-level.

This simulation mode allows targeted analysis that does not employ any cache fault tolerance policy.

- Using a practical design factor (M) to estimate the finer word size of Hamming error correction code in a cache with high failure rate. This M factor estimates according to the improvement in the fault tolerance capability in cache and the extra parity bits imposed to implement this technique. It was demonstrated that 32-bit is the optimal word size for Hamming single error correction double error detection code in cache with cell failure rate corresponding to the impact of IPF sources in 7.5 nm and 5 nm gate length UTB-SOI device.

- An evaluation method to the effectiveness of fault tolerance techniques to cover the implications of cache cell failures on cache reliability. This method offers a high credible evaluation results because it is based on the actual error pattern incurred in the system. In this thesis, it was proven that the evaluation of cache reliability using fault tolerance techniques with high ability to handle faulty words with multi faulty bits (such as Hamming triple error detection technique) will not be accurate unless by using this method.

- A case study that demonstrates the simulation of the influence of IPF sources in L1 data cache based nanometer scale UTB-SOI MOSFETs on reliability and yield of general-purpose microprocessor and how the perceptions captured can indicate a more robust L1 cache fault tolerance technique.

1.5 Thesis Outline

Chapter 2 provides the literature review for different research areas covered in this thesis. The chapter starts by introducing the concept of intrinsic parameter fluctuation (IPF), the main sources of IPF in UTB-SOI device which include : random discrete dopants in device source/drain regions, body thickness variation, and line edge roughness. The next section of the chapter overviews the implications of IPF on 6T SRAM cell scalability, emphasizes on the effects on exacerbating the cell failure in cache system, as well as, the sensitivity of L1 data cache robustness to cell failures exacerbation. Then, it reviews the present methodologies which characterize the impacts of IPF at device-level and evaluate their implications on cache at circuit and system levels.

Chapter 3 focuses on implementing the proposed methodology to investigate the general-purpose system with L1 data cache induced by IPF. This chapter starts with describing in detail each part of the framework used to implement this methodology including simulation of system-level environment, modeling cache memory induced IPF sources and developing of a faults injection scheme. Next, the mechanisms employed to model L1 cache fault and defect tolerance techniques is presented. These models include hardware redundancy for the defect tolerance techniques and parity check, Hamming SECDED ECC and Hamming TED techniques for the fault tolerance techniques. The strategy of introducing the M factor proposed to determine the finest word size for optimal SECDED ECC tolerance capability with minimal cache area overhead is also discussed. The last part of this chapter introduces the well selected benchmarks to model system daily workload on the framework. These benchmarks are selected to represent this thesis objective requirement in modeling the workload for a general-purpose applications.

Chapter 4 focuses on investigating and modeling the impact of different sources of IPF in the next generations UTB-SOI devices on cache memory. It begins with presenting the probability of cell failures in cache corresponding to the individual and combinational impact of IPF sources in UTB-SOI devices with gate length 10 nm, 7.5 nm, and 5 nm. These sources includes random discrete dopants, body thickness variation, and line edge roughness. Theses results are also provided for cache designed with cell ratio β of two. All these results are adopted to model the virtual chip of the L1 data cache that to be incorporated with the developed framework. Then, using SIMICS virtual computer platform, the stress of the workload applied by the selected benchmarks on L1 data cache area are evaluated. Finally, using the proposed M factor, the finest ECC word in L1 cache under the influence of IPF in 5 nm and 7.5 nm UTB-SOI MOSFETs are selected.

Chapter 5 investigates the capability of system level tolerance techniques employed in L1 cache memory to handle the implications of the cell failures induced by different sources of IPF in UTB-SOI with 7.5 nm and 5 nm physical get length devices. This investigation started with describing the implications of the cell failures in cache data array that does not employ any fault tolerance policy. The conclusions provided here present the expected pattern of fault occurrence in L1 data cache induced by different sources of IPF in 10 nm,7.5 nm and 5 nm

UTB-SOI MOSFETs. These sources are random discrete dopants, body thickness variation, and line edge roughness, as well as the combined impact of all these sources. The tolerance capability of hardware redundancy, parity check, SECDED ECC, and TED to keep L1 data cache function reliably under the stress of all the benchmarks workload is evaluated. This evaluation is for L1 data cache with cell failures corresponding to the impact of the effective sources of IPF in 7.5 nm and 5 nm UTB-SOI device. These sources are random discrete dopants in 7.5 nm UTB-SOI and for 5 nm UTB-SOI are random discrete dopants, and line edge roughness. The evaluation for the L1 data cache with cell failures induced by the combined of all IPF sources in 7.5 nm and 5 nm UTB-SOI are also provided. The conclusions provided concentrates on the tolerance capability and the imposed losses in CPU performance. Next, the comparison between combining of hardware redundancy with either parity check or SECDED ECC techniques in cache with cell failures induced by each effective sources of IPF in 5nm and 7.5 nm UTB-SOI device are presented. The results for the combined of all IPF sources in 7.5 nm and 5 nm are also provided. Then, this chapter investigates the tolerance capability and performance loss in L1 data cache employed hardware redundancy technique with either SECDED ECC or TED to reliably control the implications of IPF effective sources in 5 nm and 7.5 nm UTB-SOI devices. Finally, the conclusions based on the yield study that evaluates the ability of these tolerance techniques in handling the implications of the individual and combined sources of IPF are presented. The foregoing investigations was performed with cache designed with cell ratio β of two as well.

Chapter 6 concludes the findings of this research and suggests possible future work that can extend the opportunities of handling the effects of IPF in next generation MOSFETs microprocessors and systems.

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