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UNIVERSITI PUTRA MALAYSIA

CMOS VARIABLE GAIN LOW NOISE AMPLIFIER FOR RADIO FREQUENCY APPLICATIONS

LEE LINI @ LINI LEE

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By

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirement for the Degree of Doctor of Philosophy

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DEDICATIONS

"To my family members especially my beloved husband and my ever-encouraging parents for their love and support."

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the degree of Doctor of Philosophy

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November 2008

Chairman: **Roslina Mohd Sidek, PhD**

Faculty: **Engineering**

The evolution of wireless telecommunication systems is expanding in an unprecedented way and such developments have prompted many design challenges specifically for low cost and low power System-on-Chip (SoC). In order to fulfill these needs, the design challenges need to be seen from all levels of the wireless system design from architecture, circuit and the process technology. The first stage of a receiver is the radio frequency (RF) input with low noise amplifier (LNA) as the first building block. Hence, it dominates the performance of the receiver system especially in noise and sensitivity. An LNA which incorporates a variable gain stage is useful in the receiver system in order to achieve continuous gain controllability which can be used to prevent saturation in the receiver when the input signal becomes relatively large compared to the power supply. Thus, circuit solutions of current mirror, gain control loop, capacitively coupled scheme and parallel inter-stage resonance are proposed. On-chip inductors are needed in a LNA to fulfill its requirements of noise and input matching. Therefore, spiral inductors are designed, analyzed and implemented according to the specifications.

The main key part of this thesis describes the designs of the variable gain LNA (VGLNA) for low power consumption, continuous gain control and high selectivity over a wide frequency band with the target applications of frequency band at 2.0, 2.4, 5.0, 5.7 and 8 GHz. The VGLNA utilizes current mirror which allows precise copying of the current independent of temperature. With an adequate biased voltage applied, continuous gain control of approximately 28 dB is achieved at low current without degrading the noise performance of the VGLNA significantly, maintaining it below 2 dB. Second approach proposes the capacitively coupled LNA which ensures that the minimum required voltage supply for this topology is only one threshold voltage and not doubled the amount though it is a cascode transistors structure. Hence with these two innovative approaches, the power dissipation of the LNA would be minimal. Continuous gain control is achieved with the gain control loop and current mirror methods. By introducing a simple gain control loop composed of a gain control transistor and a capacitor, a wide continuous gain tuning range is achieved and with the current mirror, the VGLNA has continuous controllability of the gain. A new circuit structure named parallel inter-stage resonance LNA is proposed and it offers high selectivity of gain over the 5 GHz frequency band while keeping the noise figure below 2 dB.

The simulation results meet the desired specifications and the measurement results of transistors and inductors are shown to be comparable with the analytical results. Finally, it can be concluded that the VGLNA designs have shown continuous controllable gain and low noise with low power consumption, not forgetting high selectivity over a wide frequency band.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

PENGUAT BOLEHUBAH GANDAAN CMOS BERHINGAR RENDAH UNTUK APLIKASI BERFREKUENSI RADIO

Oleh

LEE LINI @ LINI LEE

November 2008

Pengerusi: **Roslina Mohd Sidek, PhD**

Fakulti: **Kejuruteraan**

Evolusi bagi sistem telekomunikasi wayarles sedang berkembang dengan cara yang tidak pernah berlaku dahulu dan perkembangan seperti ini telah membangkitkan pelbagai cabaran rekabentuk terutamanya bagi Sistem-dalam-Cip (SoC) yang berkos dan berkuasa rendah. Demi memenuhi keperluan ini, cabaran untuk rekabentuk perlu dicungkil daripada semua tahap rekabentuk sistem wayarles, umumnya daripada seni bina, litar dan teknologi proses. Peringkat pertama di dalam satu penerima adalah input berfrekuensi rendah dengan penguat berhingar rendah (LNA) sebagai blok pembinaan pertama. Oleh itu, ia menguasai prestasi sistem penerima tersebut terutamanya dalam bidang hingar dan kepekaan. Satu LNA yang merangkumi peringkat bolehubah gandaan adalah amat berguna di dalam sistem penerima demi mencapai kawalan gandaan berterusan yang boleh digunakan untuk mengelak ketepuan di dalam penerima apabila isyarat input menjadi terlalu besar berbanding dengan bekalan kuasa. Oleh itu, penyelesaian litar yang dicadangkan adalah arus cermin, gelung kawalan gandaan, skema terganding berkemuatan dan salunan selari antara peringkat. Induktor dalam cip

adalah diperlukan di dalam satu LNA untuk memenuhi keperluan hingar dan padanan input. Oleh itu, induktor pilin telah direkabentuk, dianalisa dan dilaksanakan mengikut spesifikasi.

Bahagian terpenting di dalam tesis ini menghuraikan rekabentuk LNA bolehubah gandaan (VGLNA) untuk penggunaan kuasa rendah, kawalan gandaan berterusan dan pemilihan tinggi pada jalur frekuensi yang lebar serta juga dengan sasaran aplikasi pada jalur frekuensi 2.0, 2.4, 5.0, 5.7 dan 8.0 GHz. VGLNA menggunakan arus cermin bagi salinan tepat untuk arus tanpa dipengaruhi oleh suhu. Beserta dengan nilai voltan terpincang yang sesuai, kawalan gandaan berterusan bernilai lebih kurang 28 dB boleh diperolehi pada arus yang rendah tanpa merendahkan prestasi hingar VGLNA secara nyata sekali dengan mengekalkan nilai hingar di bawah 2 dB. Cara kedua mencadangkan LNA terganding berkemuatan yang memastikan bahawa bekalan voltan minima yang diperlukan bagi topologi ini hanyalah satu voltan ambang dan bukannya dua walaupun ia merupakan satu struktur transistor kaskod. Dengan dua cara inovatif ini, pelepasan kuasa pada LNA adalah minima. Kawalan gandaan berterusan boleh dicapai melalui gelung kawalan gandaan dan arus cermin. Melalui gelung kawalan gandaan yang dibina daripada satu transistor kawalan gandaan dan juga satu pemuat, satu julat penalaan gandaan berterusan yang lebar boleh diperolehi. Tambahan pula, dengan menggunakan arus cermin, litar VGLNA akan mempunyai pengawalan gandaan yang berterusan. Satu struktur litar yang baru bernama salunan selari antara peringkat telah dicadangkan dan ia memberi pemilihan yang tinggi bagi gandaan pada jalur frekuensi 5 GHz serta mengekalkan hingar pada nilai kurang daripada 2 dB.

Keputusan simulasi menunjukkan bahawa VGLNA memenuhi spesifikasi yang dikehendaki dan keputusan ukuran bagi transistor dan inductor menunjukkan hasil yang setara dengan keputusan analitikal. Akhirnya, ini boleh disimpulkan bahawa rekabentuk VGLNA telah menunjukkan kawalan gandaan berterusan dan hingar rendah dengan penggunaan kuasa rendah, serta memberi pemilihan yang tinggi pada satu jalur frekuensi yang lebar.

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I certify that a Thesis Examination Committee has met on 6th November 2008 to conduct the final examination of Lee Lini @ Lini Lee on her thesis entitled "CMOS Variable Gain Low Noise Amplifier For Radio Frequency Applications" in accordance with Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U (A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee are as follows:

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Date: 12 February 2009

DECLARATION

I declare that the thesis is my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously, and is not concurrently, submitted for any other degree at Universiti Putra Malaysia or at any other institution.

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LEE LINI @ LINI LEE

Date: 2 December 2008

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Abbreviations

3G	Third Generation
4G	Forth Generation
AC	Alternating current
ADC	Analog-to-digital converter
ADS	Agilent's Advanced Design System program
AGC	Automatic gain control
AM	Amplitude modulation
ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for ICs
BB	Baseband
BER	Bit error rate
CMOS	Complementary Metal Oxide Semiconductor
CG	Common-gate
CP	Compression point
DAC	Digital-to-analog converter
DC	Direct Current
DCR	Direct Conversion Receiver
DCS	Digital Communication System
DECT	Digital Enhanced Cordless Telecommunications
DRC	Design Rule Check
DS-CDMA	Direct Sequence Code Division Multiple Access
DSP	Digital Signal Processing
DUT	Die Under Test

EDGE	Enhanced Data rates for GSM Evolution
ESD	Electrostatic Discharge
F	Noise factor
FM	Frequency modulation
GDSII	Gerber Data Stream Information Interchange
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSG	Ground-Signal-Ground
GSM	Global System for Mobile Communications
HGM	High gain mode
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IEEE-ISA	Institute of Electrical and Electronics Engineers – International Standards Association
IF	Intermediate Frequency
IIP3	Input-referred third order intercept point
IM3	Third order intermodulation
IMT-2000	International Mobile Telecommunications in the year 2000
IP3	Third order intercepts point
ISM	Industrial, Scientific and Medical
ISS	Impedance Standard Substrate
LC-tank	A parallel circuit consists of an inductor and a capacitor
LGM	Low gain mode
LNA	Low noise amplifier
LO	Local oscillator
LPF	Low pass filter

LVS	Layout versus schematic
MIMO	Multiple Input – Multiple Output
NF	Noise Figure
NFA	Noise Figure Analyzer
OFDM	Orthogonal Frequency-division Multiplexing
P1dB	1-dB Gain Compression Measurement
PCN	Personal Communication Network
PCS	Personal Communication Services
PDA	Personal Digital Assistance
PSS	Periodic Steady-State
RC-CR	Resistive and capacitive
RF	Radio Frequency
SA	Spectrum Analyzer
SAW	Surface Acoustic Wave
SDF	Spectral Density Function
SMU	Source measure unit
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SOLT	Short-Open-Load-Through
U-NII	Unlicensed National Information Infrastructure
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier

VGLNA	Variable gain low noise amplifier
VNA	Vector Network Analyzer
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Networks