DEVELOPMENT OF A FUNCTIONAL DIGITAL INTEGRATED CIRCUIT TESTING SYSTEM USING MIXED-MODE TECHNIQUE

By

MD. LIAKOT ALI

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirements for the Degree of Doctor of Philosophy

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DEDICATION

This Thesis is dedicated
to

My Parents
Late Md. Abubaker Sheikh and Mrs. Shaharon Nesa

My Brothers
Md. Mahbubur Rahman, Abdul Quddus, Dr. Wadud and Dr. Shawkat

&

My Wife
Umme Salma

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment of the requirements for the degree of Doctor of Philosophy

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Chairman: **Roslina Sidek, Ph.D.**

Faculty: **Engineering**

With the continuous increase in design complexities and packing densities of integrated circuit (IC), problems associated with conventional Automatic Test Equipment (ATE)-based IC testing approach have become a burning issue in the semiconductor world, which needs an economic solution with reliable performance. Recently, the superiority of Dynamic Reseeding-based Mixed-mode (DRM) technique has been proven over all other existing test techniques in the Built-in Self-Test (BIST) environment. This thesis introduces the implementation of the DRM technique in a system-on-a-chip (SOC) in alleviating the problems of conventional ATE-based external testing of digital IC. The performance of the SOC in IC testing has been verified using fault simulation experiments on the ISCAS85 benchmark circuits (Circuits proposed in the International Symposium on Circuits and Systems in 1985). Significant improvement is observed in achieving complete fault coverage for the ISCAS85 benchmark circuits using acceptable number of test vectors. Fault simulation results show that the proposed DRM technique produces 100% fault coverage for the benchmark circuits c432, c1355, c1908, c2670, c3540 and c5315

using the 232, 526, 996, 336, 360 and 748 test cubes, respectively which are much lower than the numbers from the approaches suggested by other researchers. It also offers much lower data storage requirements in IC testing than the conventional ATE-based testing approach. The results show that 2 to 11 times less memory is needed for testing the ISCAS85 benchmark circuits using the DRM technique than that of the deterministic testing approach.

Verilog Hardware Description Language (HDL), which is an industry standard IC design tool, has been used to design the SOC proposed in this thesis. Main modules of the SOC are micro-UART (Universal Asynchronous Receiver and Transmitter), a controller, pattern generator, signature analyzer (SA), instruction registers and Random Access Memories (RAMs). A prototype test set-up has been developed for testing IC by implementing the design of the SOC into a Field Programmable Gate Array Logic (FPGA) chip and then by interfacing the FPGA chip with a personal computer (PC) through a Graphical User Interface (GUI). For testing a circuit, necessary test information is loaded into the SOC and the testing process is executed using the GUI from the PC. The SOC goes into autonomous mode. It generates test vectors, applies them to the Circuit Under Test (CUT) and captures the output responses and sends it into the SA for compression. At the end of testing, the generated signature is compared with that of a reference circuit (fault-free circuit of the same type) and the CUT is identified as fault-free if the two signatures are the same and as faulty if otherwise. The operation of the SOC has been verified in real time by testing a 16-bit multiplier as a sample CUT. It is user programmable, which increases flexibility and reliability in IC testing. It is capable of testing functionality of combinational circuits as well as sequential circuits with scan-path facility.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

PEMBANGUNAN SEBUAH SISTEM PENGUJIAN FUNGSI LITAR BERSEPADU DIGIT MENGGUNAKAN TEKNIK MOD CAMPURAN

Oleh

MD. LIAKOT ALI

Oktober 2004

Pengerusi: Roslina Sidek, Ph.D.

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Dengan bertambahnya kesukaran rekabentuk dan kepadatan pembungkusan litar bersepadu, masalah berkaitan dengan pendekatan pengujian litar bersepadu berasaskan Ujian Peralatan Automatik (ATE) yang lazim telah menjadi suatu isu yang membebankan di dalam dunia semikonduktor, di mana ia berkehendakan penyelesaian yang ekonomi dengan prestasi yang boleh diharapkan. Baru-baru ini, kelebihan teknik Mod Campuran Berasaskan Pembenihan Semula Dinamik (DRM) telah dibuktikan mengatasi kesemua teknik-teknik pengujian yang wujud di dalam persekitaran Penguji Terbina Dalam (BIST). Tesis ini mengenalkan perlaksanaan teknik DRM di dalam sistem di atas cip (SOC) untuk mengatasi permasalahan penguji litar bersepadu yang berdasarkan ATE yang lazim. Persembahan SOC ini di dalam pengujian litar bersepadu telah disahkan menggunakan pengujian penyelakuan kerosakan ke atas litar-litar penanda aras ISCAS85 (Litar-litar ini dicadangkan di dalam Simposium Antarabangsa Litar dan Sistem dalam tahun 1985). Kelebihan yang ketara diperhatikan di dalam pencapaian penuh liputan kerosakan bagi litar-litar penanda aras ISCAS85 mengunakan jumlah bilangan vektor-vektor pengujian yang

boleh diterima. Keputusan penyelakuan kerosakan menunjukkan teknik DRM yang dicadangkan menghasilkan 100% rangkuman kegagalan untuk litar-litar penanda aras c432, c1355, c1908, c2670, c3540 dan c5315 dengan menggunakan 232, 526, 996, 336, 360 dan 748 kubah-kubah ujian, yang mana ianya lebih rendah daripada pendekatan yang dicadangkan oleh penyelidik-penyelidik lain. Ia juga memerlukan penyimpanan data yang lebih rendah dalam pengujian litar bersepadu daripada pendekatan pengujian berdasarkan ATE yang lazim. Keputusan menunjukkan 2 hingga 11 kali lebih rendah memori diperlukan untuk menguji litar-litar penanda aras ISCAS85 menggunakan teknik DRM berbanding pendekatan pengujian yang tertentu.

Bahasa Perihalan Perkakasan Verilog (HDL) iaitu perkakas rekabentuk litar bersepadu industri yang piawai telah digunakan untuk merekabentuk SOC yang dicadangkan di dalam tesis ini. Modul SOC yang utama ialah micro-UART ("Universal Asynchronous Receiver and Transmitter"), sebuah alat kawalan, penjana corak, penganalisa tandatangan (SA), daftar-daftar ajaran dan Ingatan-ingatan Capaian Rawak (RAMs). Sebuah contoh ulung penguji litar bersepadu dibina dengan melaksanakan rekabentuk SOC ke dalam cip Tatasusunan GET Boleh Atur Caraan Medan (FPGA) dan mengantaramukakannya dengan komputer peribadi (PC) melalui pengguna antaramuka grafik yang mesra pengguna (GUI). Bagi menguji CUT, maklumat yang perlu dimuatkan ke dalam SOC dan proses pengujiannya dilaksanakan menggunakan GUI dari PC. SOC bertindak dalam mod pergerakan sendiri (berautonomi). Ia menjana vektor-vektor penguji, menggunakan vektor-vektor tersebut ke atas Litar Di bawah Ujian (CUT) serta menangkap sambutan keluaran dan menghantar ke penganalisa tandatangan (SA) untuk pemampatan. Pada

akhir pengujian tandatangan yang dijana dibandingkan dengan sebuah litar rujukan (litar yang bebas kerosakan yang sama jenis) dan CUT itu dikenalpasti sebagai bebas dari kerosakan sekiranya kedua-dua tandatangan adalah sama, dan sebagai rosak jika sebaliknya. Operasi SOC telah disahkan dalam masa nyata dengan menguji pendarab 16-bit sebagai sampel CUT. Ia boleh diaturcara oleh pengguna yang mana meningkatkan keanjalan dan juga keboleharapannya di dalam pengujian litar bersepadu. Ia berkebolehan menguji litar-litar gabungan dan litar-litar jujukan dengan kemudahan laluan imbas. Ia boleh digunakan untuk menguji sebuah litar CUT yang diletakkan atas sekeping papan litar bercetak (PCB) sekiranya CUT tersebut mempunyai kemudahan laluan imbas.

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I certify that an Examination Committee met on 28th October 2004 to conduct the final examination of Md. Liakot Ali, on his Doctor of Philosophy thesis entitled "Development of a Functional Digital IC Testing System using Mixed-mode Technique" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

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MD. LIAKOT ALI

Date:

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