



**UNIVERSITI PUTRA MALAYSIA**

**THE DESIGN OF LOW POWER CMOS SRAM SUBSYSTEMS**

**LEE CHU LIANG**

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**THE DESIGN OF LOW POWER CMOS SRAM SUBSYSTEMS**

**By**

**LEE CHU LIANG**

**Thesis Submitted in Fulfilment of the Requirement for the  
Degree of Master of Science in the Faculty of Engineering  
Universiti Putra Malaysia**

**June 2001**



Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfilment  
of the requirement for the degree of Master of Science

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**LEE CHU LIANG**

**June 2001**

**Chairman : Encik Rahman Wagiran**

**Faculty : Engineering**

The low power circuit design technique has been the trend in developing portable and smaller size electronic products, especially for communication peripherals. In the limitation on the device technology, integrated circuit design work has played an important role in performing various low power techniques. This thesis presents the design of low power Complementary Metal Oxide Semiconductor (CMOS) Static Random Access Memory (SRAM) Subsystems. CMOS technology performs much lower static power dissipation compares to other technologies. The implementation of this design by using 3.3 V supply voltage has effectively reduced the dynamic power dissipation of the circuitry. Low power is achieved by implementing 6T-memory cell. Low power techniques are also achieved on capacitance reduction by using divided word-line structure for address decoder. Finally the low power is achieved by the operating voltage reduction using current-mode sensing technique for sense amplifier with the pre-charge voltage of  $V_{dd}/2$ .

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia  
Sebagai memenuhi keperluan untuk ijazah Master Sains

**REKABENTUK CMOS SUBSISTEM SRAM BERKUASA RENDAH**

**Oleh**

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Teknik rekabentuk untuk litar berkuasa rendah telah menjadi satu amalan dalam pembangunan barangan elektronik yang mudah alih dan bersaiz kecil terutamanya bagi alat komunikasi. Semakin teknologi peranti mencapai hadnya, rekabentuk litar bersepadu menjadi semakin penting dalam usaha untuk mempelbagaikan teknik untuk litar berkuasa rendah. Tesis ini akan menyampaikan rekabentuk Complementary Metal Oxide Semiconductor (CMOS) Subsistem Static Random Access Memory (SRAM) berkuasa rendah. Teknologi CMOS kurang kehilangan kuasa statik berbanding dengan teknologi lain. Implementasi rekabentuk litar ini dijalankan dengan menggunakan 3.3V sebagai sumber voltan yang telah secara berkesan mengurangkan kehilangan kuasa dinamik litar tersebut. Kuasa rendah boleh dicapai dengan menggunakan sel ingatan 6T. Teknik berkuasa rendah juga boleh dicapai menggunakan pengurangan kapasitan dengan menggunakan struktur pembahagi baris untuk pengkodan alamat. Akhirnya kuasa rendah boleh dicapai dengan pengurangan voltan operasi dengan menggunakan teknik pengesan secara mod arus untuk penguat-kesanan dengan pra-cas bervoltan  $V_{dd}/2$ .

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Lastly, I would like to express my sincere appreciation to my family for their undying love, patience and supports which have enable me to complete the project successfully.


I certify that an Examination Committee met on 15<sup>th</sup> June 2001 to conduct the final examination of Lee Chu Liang on his Master of Science thesis entitled “The Design of Low Power CMOS SRAM Subsystems” in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulation 1981. The committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committees are as follows:

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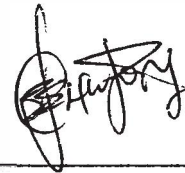
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## DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.



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## TABLE OF CONTENTS

	<b>Page</b>
<b>ABSTRACT</b>	ii
<b>ABSTRAK</b>	iii
<b>ACKNOWLEDGEMENTS</b>	iv
<b>APPROVAL SHEETS</b>	v
<b>DECLARATION FORM</b>	vii
<b>LIST OF TABLES</b>	x
<b>LIST OF FIGURES</b>	xi
<b>LIST OF ABBREVIATIONS</b>	xiv
<b>CHAPTER</b>	
<b>1 INTRODUCTION</b>	
The Design of Low Power SRAM .....	1
Circuit Limitation of Low Power VLSI Design .....	5
Objective of This Work .....	6
Thesis Organization .....	7
<b>2 LITERATURE REVIEW</b>	
CMOS Technology .....	8
Development of Low Power SRAM .....	9
Address Decoder .....	10
Sense Amplifier .....	11
Conclusion .....	12
<b>3 METHODOLOGY</b>	
General Overview .....	13
CMOS Technology and Simulation Tools .....	14
Power Dissipation in CMOS Circuit .....	15
Static Power Dissipation .....	15
Dynamic Power Dissipation .....	16
Power Dissipation by using Simulation Tool .....	20
Digital Gate Design .....	21
Cascade Buffer Design .....	22
Input Capacitance .....	25
Propagation Delay and Rise/ Fall Time .....	27
Voltage Transfer Curve .....	29
Latch-up Prevention .....	30



SRAM Subsystems Architecture .....	32
Memory Cell .....	32
Address Decoder .....	39
Sense Amplifier .....	45
<b>4 RESULTS AND DISCUSSION</b>	
Memory Cell .....	48
The Comparison of 4-T and 6-T SRAM Cell .....	48
6T Memory Cell Transistor Sizing .....	50
Address Decoder .....	56
Digital Gates and Fan-in .....	56
Cascaded Buffer .....	57
Row Decoder .....	62
Column Decoder .....	71
Sense Amplifier .....	74
The Comparison of Voltage Sense Amplifier and Current Sense Amplifier .....	74
Transistor Sizing and Power Dissipation .....	77
Read/ Write and Sensing Operation .....	80
<b>5 CONCLUSION</b>	
Memory Cell .....	87
Address Decoder .....	88
Sense Amplifier .....	89
Conclusion .....	90
<b>REFERENCES</b> .....	92
<b>APPENDICES</b>	
<b>A Model file of <i>MOSIS/ ORBIT 2.0<math>\mu</math>m SCNA technology,</i></b> <b>Level 2 MOSFET</b> .....	94
<b>B Design Rules for <i>MOSIS/ ORBIT 2.0<math>\mu</math>m N-Well (SCNA)</i></b> <b><i>Technology</i></b> .....	95
<b>C Partial Pattern Scheme for <i>MOSIS/ ORBIT 2.0<math>\mu</math>m N-Well</i></b> <b><i>(SCNA) technology</i></b> .....	96
<b>BIODATA OF AUTHOR</b> .....	97

## LIST OF TABLES

<b>Table</b>		<b>Page</b>
4.1	Comparison of transistors channel width for 6T memory cell.	51
4.2	Results of calculated parameters in cascaded buffer. ....	62
4.3	Results summary of propagation delay for decoder blocks. ....	69
4.4	Output rise time and fall time of decoder blocks. ....	70
4.5	Propagation delay and rise / fall time for column decoder input gates and cascaded buffer. ....	73
4.6	Comparison of transistor's channel width for Current Sense Amplifier. ....	77
4.7	Propagation delay and rise / fall time for Current Sense Amplifier. ....	79

## LIST OF FIGURES

Figure	Page
1.1 Floorplan of 512 x 8-bits low power SRAM subsystems .....	2
1.2 Design Flow using Tanner Tools. ....	4
2.1 Gate delay versus power consumption of various logic families.	8
3.1 Model describing parasitic diodes present in a CMOS inverter.	16
3.2 Charge sharing in CMOS dynamic circuit. ....	19
3.3 Input switching waveform and model for short-circuit current.	20
3.4 Cascaded buffer for driving large capacitive loads. ....	23
3.5 MOS cross section showing parasitic capacitance. ....	26
3.6 Switching characteristic for CMOS circuit. ....	29
3.7 CMOS VTC and noise margin definitions diagram. ....	30
3.8 The origin model of CMOS Latch-up. ....	31
3.9 A pair of inverters forming a bistable element. ....	32
3.10 VTC of a latch. ....	33
3.11 (a) Six transistors SRAM cell (b) Four transistors SRAM cell.	34
3.12 Reading data from 6T cell. ....	35
3.13 Writing for a $Q = 0$ with 1 previously stored. ....	37
3.14 Transistor M6 discharging node Q while fighting the p-channel pull-up M4 modeled as a resistor. ....	38
3.15 Divided word-line (DWL) structure in SRAM. ....	41
3.16 DWL architecture of the row decoding structure. ....	42
3.17 Local Word Decoder architecture. ....	43

3.18	2-bits CMOS pass transistor Column Decoder. ....	44
3.19	Current Sense Amplifier. ....	46
4.1	(a) 6T memory cell VTC (b) 4T memory cell VTC. ....	49
4.2	Layout of 6T memory cell with size of 39.0 $\mu$ m x 85.5 $\mu$ m. ....	52
4.3	6T memory cell extracted net-list file. ....	52
4.4	VTC from layout net-list file. ....	53
4.5	Power dissipation output file from layout net-list extraction. ....	53
4.6	Layout of an inverter. ....	56
4.7	Layout of a 2-input NAND gate. ....	57
4.8	Layout of word-line buffer. ....	58
4.9	Layout of global row decoder buffer. ....	59
4.10	Layout of pass transistor buffer. ....	60
4.11	Layout of block-select buffer. ....	61
4.12	Layout of Pre-decoder. ....	63
4.13	(a) Transient analysis of Pre-decoder for address signal X0 (b) Transient analysis of Pre-decoder for address signal X1 (c) Transient analysis of Pre-decoder for gated address signal X2 and X3. ....	64
4.14	Layout of global word decoder. ....	65
4.15	(a) Transient analysis of GWD for address signal X0 (b) Transient analysis of GWD for gated address signal X1 and X2X3. ....	66
4.16	Layout of half side of the local word decoder with eight rows of memory cell array. ....	67
4.17	Transient analysis of LWD for gated address signal X0 and X1-X3. ....	67
4.18	Block diagram of row decoders in layout. ....	70

4.19	One unit column of CMOS pass transistor with memory cell.	71
4.20	Layout of a group of pass transistors with cascaded buffer and memory cells. ....	72
4.21	Transient analysis of column decoder input gates and pass transistor buffer. ....	73
4.22	Partial extracted layout net-list file showing parasitic capacitance of output DB (oa) and output /DB (ob). ....	74
4.23	Double-ended Current-mirror Differential Amplifier. ....	75
4.24	Transient analysis of current sense amplifier and double-ended current-mirror differential amplifier for 1.4V difference in input voltage. ....	75
4.25	Transient analysis of current sense amplifier and double-ended current-mirror differential amplifier for 0.5V difference in input voltage. ....	76
4.26	Layout of Current Sense Amplifier. ....	78
4.27	Power dissipation output file from layout net-list extraction. ....	80
4.28	Schematic describing the read and write sensing operation circuit.	81
4.29	SPICE simulation net-list describing the analysis and circuit for read and write operation. ....	82
4.30	(a) Read operation transient analysis, internal nodes. (b) Read operation transient analysis, output sense. ....	83
4.31	Write and Pre-charge Operation. ....	85
4.32	Write a Q=0 with 1 previously stored. ....	85



## LIST OF ABBREVIATIONS

4T cell	Four transistors memory cell
6T cell	Six transistors memory cell
$C_d$	Drain capacitance
$C_g$	Gate capacitance
$C_L$	Load capacitance
$C_{ox}$	Capacitance oxide
CMOS	Complementary Metal Oxide Semiconductor
DWL	Divided Word-Line
Gnd	Ground
GWD	Global Word Decoder
$I_D$	Drain current
$K_n$	NMOS Transconductance coefficient
$K_p$	PMOS Transconductance coefficient
L	Channel Length
LWD	Local Word Decoder
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-channel Metal Oxide Semiconductor
PMOS	p-channel Metal Oxide Semiconductor
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
$V_{DS}$	Drain-source voltage
$V_{GS}$	Gate-source voltage
$V_{dd}$	Supply voltage
VTC	Voltage Transfer Curve
$V_t$	MOSFET Threshold voltage
W	Channel Width
$\beta$	Taper factor
$\beta_{eff}$	MOSFET process gain factor
$\tau$	Time constant



## **CHAPTER 1**

### **INTRODUCTION**

#### **The Design of Low Power SRAM**

The low power Static Random Access Memory (SRAM) integrated circuit design technique has always been the trend in developing portable electronic products. With the demand on reducing weight and size of portable system, instead of miniaturizing the batteries, designing low power digital systems has become a more practical step. With memory accounting for the largest share of power consumption in a system, circuits designing techniques are a leading field with device technology constraint.

SRAM is a volatile memory in which data in the memory will disappear when power supply is turned off. A latch structure is used in the SRAM memory cell to store data. More transistors are needed in the SRAM memory cell compare with a DRAM which is based on dynamic storage of charge for data storage. Today's industry uses SRAM especially as memory cache mainly because of its speciality in high speed for read and writes operations.

Figure 1.1 shows the floorplan of the SRAM subsystems design in this work. The memory cell arrays are divided into four similar portions with modules in between. Pre-decoder and global row decoders are placed in the center column.



Column decoders, sense amplifier, write drivers and I/O buffers are placed in the center horizontal area.

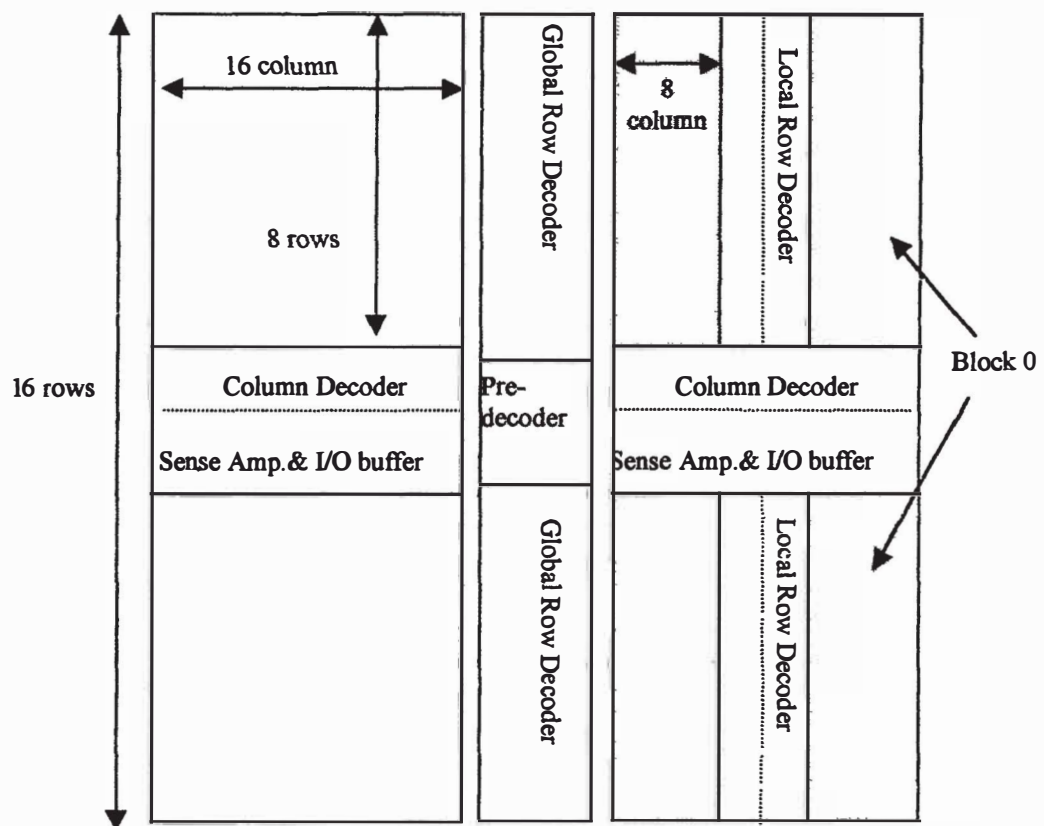


Figure 1.1: Floorplan of 512 x 8-bits low power SRAM subsystems.

The emphasis on this work is mainly on the design of memory cell, address decoder and the sensing amplifier. For each of these subsystems, low power techniques have been reviewed and the suitable techniques are adopted in this work.

Low power consideration will subsequently lead to the deterioration of the system performance especially in delay parameter. Since the main justification for the existence of the SRAM is its speed, thus the low-power circuit design techniques used in this work are to be concerned and compromised with its high-speed performance. The design work is carried out using Tanner Tools Pro. using SPICE simulation. The design flow is shown in Figure 1.2. The design work of the 512 x 8-bits low density SRAM subsystems has indeed a great gain in obtaining basic knowledge of circuit design skills and techniques. The variety of proposed circuit design techniques in designing the low power SRAM Subsystems has also a perfect reference for a beginner to step in the world of art of the integrated circuit design.

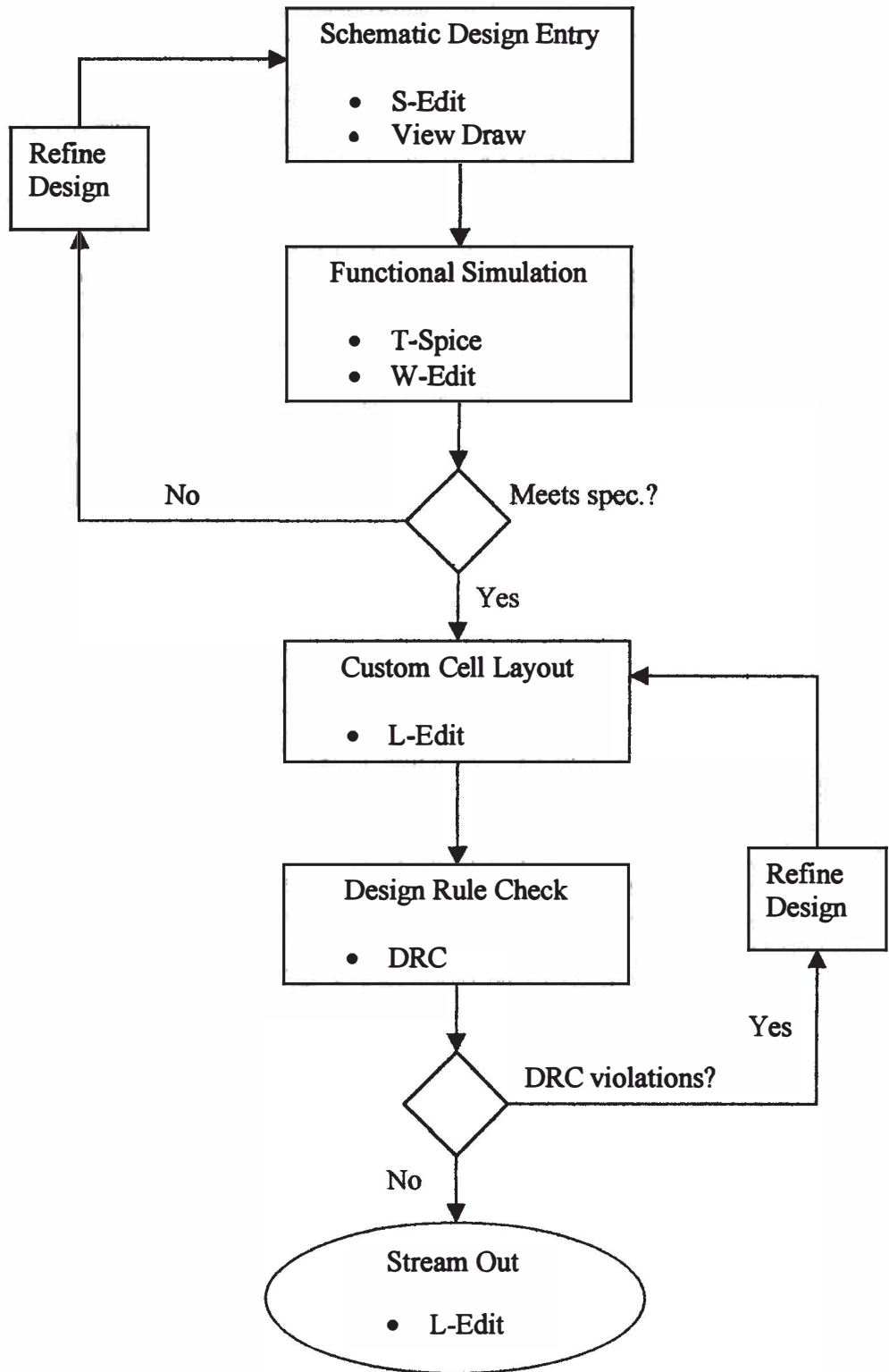


Figure 1.2: Design Flow using Tanner Tools

## Circuit Limitation of Low Power VLSI Design

The circuit level limits are independent of the architecture of a particular system. There are a few circuit level limits for CMOS technology. The first generic circuit limit is the supply voltage. Reducing supply voltage is the most effective way of decreasing dynamic power dissipation in CMOS circuit. However the minimum supply voltage is determined by the minimum threshold voltage by a simple equation (Luo and Kuo,1999) which is

$$V_{dd,min} = 3V_{T,min} \quad \dots 2.1$$

In this work, lower voltage 3.3 V is chosen instead of 5 V. With reference to the available technology model file, supply voltage 3.3 V still fulfills the requirement of the Equation 2.1. Further more, lower power supply voltage will significantly reduce the speed of operation. This is because the increase in the gates' transition time is inversely proportional to the supply voltage, as in Equation 2.2. where k is the process constant,  $\beta_{p/n}$  is the process gain factor and  $C_L$  the load capacitance.

$$t_{r/f} = k \left( \frac{C_L}{\beta_{p/n} V_{dd}} \right) \quad \dots 2.2$$

The second generic circuit limit is the switching frequency. The dynamic power dissipation is

$$P = \frac{1}{2} C_L V_{dd} f \quad \dots 2.3$$

The highest frequency devices are used but operating them at the lowest possible frequency.

The third limitation is on the intrinsic gate delay that is the time taken to charge or discharge the load capacitance. With the available technology model file, this problem can be overcome by using less fan-out with minimum geometry.

### **Objective of This Work**

Low power techniques has been one of the challenges today in producing portable and smaller electronics products. SRAM being one of the most high power consumption products will be the first front priority to be studied. In this work, low power techniques are studied by using available technology.

The objectives of this thesis is to present the circuit design of CMOS SRAM subsystems using low power techniques and further develops its physical layout by using available Mosis/ ORBIT 2.0 $\mu$ m Level 2 CMOS technology. Implementation of this design by using 3.3 V supply voltage is to reduce the dynamic power dissipation of the whole circuitry. Studies are made on three subsystems of SRAM as below:

- a) Implementation of low power 6T-memory cell.
- b) Low power technique implementation on capacitance reduction by using divided word-line structure for address decoder.

- c) Implementation of current sense amplifier with the pre-charge voltage of  $V_{dd}/2$ .

The benefits of this design work will be the valuable knowledge and circuit design experience. In terms of contribution, this work can be a valuable learning reference in circuit level design work.

### **Thesis Organization**

This thesis comprises of five chapters. Chapter 1 gives an overview to this project being done. The limitations of the circuit level design are discussed and the objectives of this work are mentioned. Chapter 2 presents the literature review which discusses the related research work had been done previously. Chapter 3 discusses the methodology involved in this design work. The theory of the origin of power dissipation in CMOS is also presented.

The scope of this project will be captured in three subtitles in Chapter 3. These subtitles are discussing memory cell, address decoder and sense amplifier, which are three of the core part of SRAM architecture. The detail description of the technique and structures used are also presented. The results obtained are then discussed in Chapter 4. Finally, Chapter 5 will conclude the work.

## CHAPTER 2

### LITERATURE REVIEW

#### CMOS Technology

CMOS circuits have been the forefront of the technology due to their low passive power consumption. Aside from leakage currents, power in CMOS circuit is only dissipated during switching events. Virtually no power consumed when the circuit is in the steady state. Figure 2.1 shows gate delay versus power consumption of various logic families (Kohyama, 1990). At a power-delay product value, CMOS offers the smallest power-delay product among all available technology.

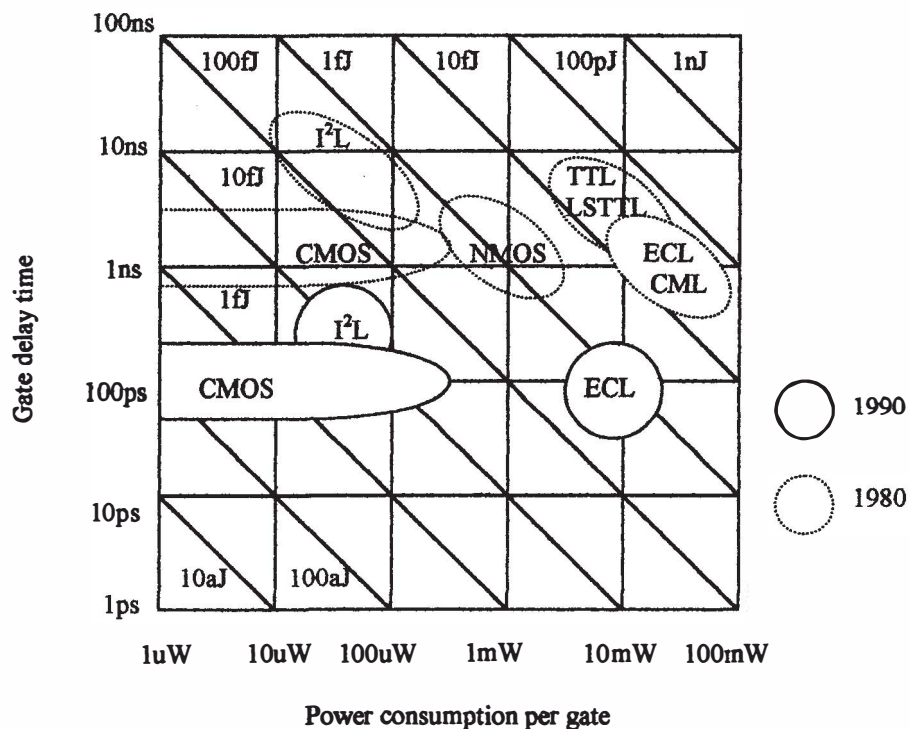


Figure 2.1: Gate delay versus power consumption of various logic families (Kohyama, 1990).

In addition, CMOS is flexible for a wide variety of design applications, which include digital logic, signal processing and a variety of analog circuits. The significant features of CMOS with its stable operation have further permitted varieties of CMOS IC to be fabricated with high yield.

As a result of today's technology, it is widely accepted that power efficiency is a design goal at par in importance with miniaturization and performance. Therefore, the practice of low power design is being adopted and dominated by the CMOS technology.

### **Development of Low Power SRAM**

Memory circuits form an integral part of every system design and significantly contributing to the system level power consumption. Two examples of recently presented reduced-power processors show that 43% and 50.3% respectively of the total system consumption is attributed to the memory circuits (Stephany et al., 1998; Igura et. al., 1998). Therefore, reducing the power dissipation in memories can significantly improve the system power-efficiency, performance, reliability and overall costs.

The main justification for the existence of SRAM is its speed since it consumes a quarter of the area capacity of DRAM for the same process technology and chip size. The bandwidth mismatch is better between microprocessor and the



SRAM than the DRAM. A rapid growing classification of fast memory architecture is the Synchronous SRAM especially used as the cache in PC systems. With the rapid development in VLSI fabrication technology that has led to the increased densities of integrated circuits with the decreased device geometry, low supply voltage have effectively reduces the excessive power dissipation and decreases run time failure and reliability problems. SRAM has experienced a very rapid development of low power design due to an increased demand for notebooks, laptops, hand-held communication devices and IC memory cards.

### **Address Decoder**

Researches had been made on the reduction of power consumed during word-line activation. Divided word-line (DWL) approach has been the most preferable because of its effectiveness in reducing load and save unused power (Yoshimoto, 1983). It is commonly used especially in an increasing density of memory array size. In the further extend of DWL architecture, the hierarchical word-line decoding (HWD) technique is used for higher density SRAM (Hirose et. al., 1990). This architecture has three layer hierarchy which includes the global word-lines, sub-global word-lines, and local word-lines. Other than this, the technique using hierarchical divided bit-line that results in the reduction in the bit-lines capacitance instead of word-lines capacitance had been presented recently (Karandikar, 1998). This architecture uses slightly different memory cell's structure in which it used single bit-line and double word-line. However, in this work, divided word-line is used due to the small density of the memory cell array.